

COMPAL CONFIDENTIAL

MODEL NAME : CDP80

PCB NO : LA-E151P

BOM P/N :

GPIO MAP: Dell GPIO map EC16 062416 Compal Only

Breckenridge 15 UMA

Kabylake H

2016-07-01

REV : 0.2 (X01)

@ : Nopop Component

EMI@ : EMI Component

@EMI@ : EMI Nopop Component

ESD@ : ESD Component

@ESD@ : ESD Nopop Component

RF@ : RF Component

@RF@ : RF Nopop Component

XDP@ : XDP Component

CONN@ : Connector Component

www.aitech1.ru

MB PCB

| Part Number | Description |
|-------------|--------------------------------|
| DA80018K000 | PCB 1SE LA-E151P REV0 MB UMA 1 |

Layout Dell logo



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REV: X01
PWB: V0RVF

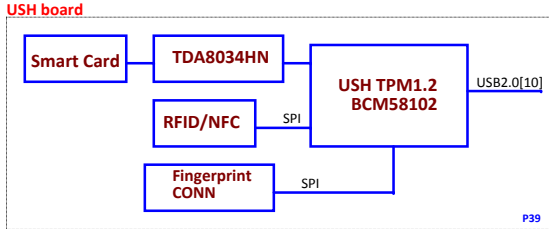
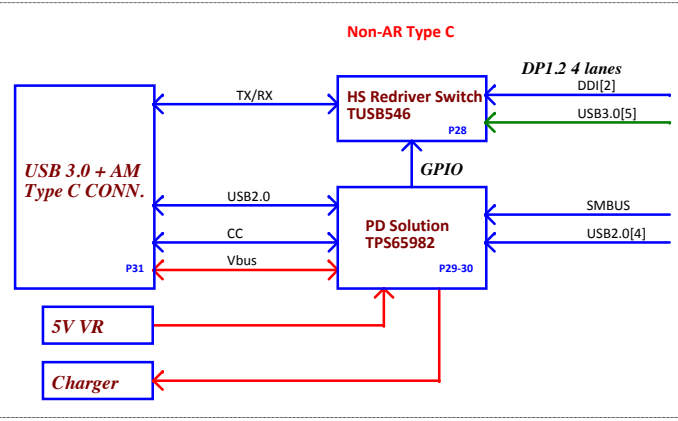
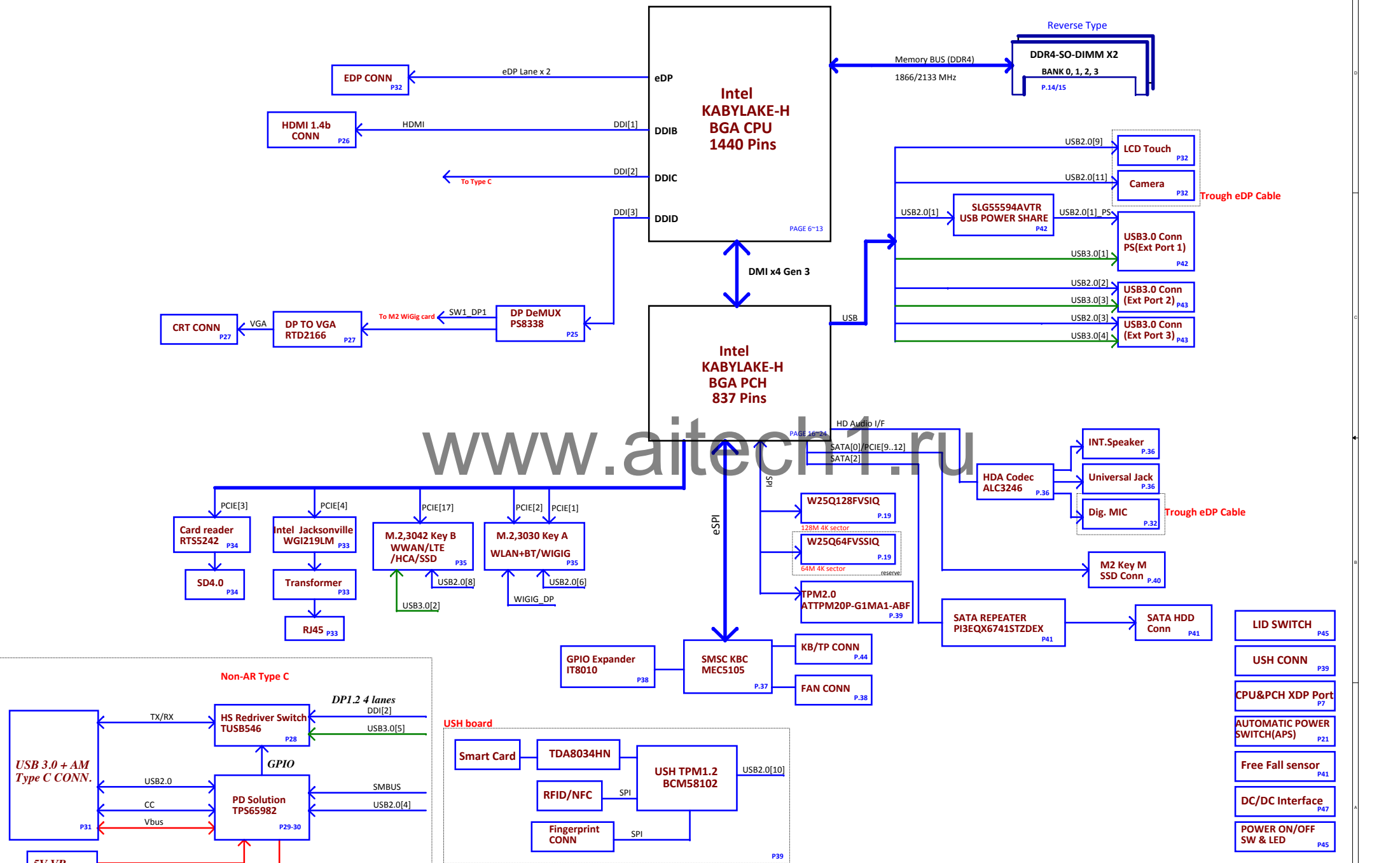
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Cover Sheet

| Security Classification | | Compal Secret Data | | Title | |
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| Date: Friday, July 01, 2016 | | | | Sheet 1 | of 61 |

Breckenridge 15 UMA non-TBT Block Diagram



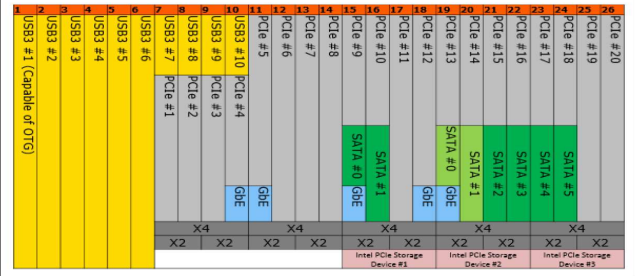
POWER STATES

| Signal State | SLP S3# | SLP S4# | SLP S5# | SLP A# | ALWAYS PLANE | M PLANE | SUS PLANE | RUN PLANE | CLOCKS |
|------------------------------|------------|------------|------------|-----------|-----------------|------------|--------------|--------------|--------|
| S0 (Full ON) / M0 | HIGH | HIGH | HIGH | HIGH | ON | ON | ON | ON | ON |
| S3 (Suspend to RAM) / M3 | LOW | HIGH | HIGH | HIGH | ON | ON | ON | OFF | OFF |
| S4 (Suspend to DISK) / M3 | LOW | LOW | HIGH | HIGH | ON | ON | OFF | OFF | OFF |
| S5 (SOFT OFF) / M3 | LOW | LOW | LOW | HIGH | ON | ON | OFF | OFF | OFF |
| S3 (Suspend to RAM) / M-OFF | LOW | HIGH | HIGH | LOW | ON | OFF | ON | OFF | OFF |
| S4 (Suspend to DISK) / M-OFF | LOW | LOW | HIGH | LOW | ON | OFF | OFF | OFF | OFF |
| S5 (SOFT OFF) / M-OFF | LOW | LOW | LOW | LOW | ON | OFF | OFF | OFF | OFF |

PM TABLE

| power plane State | +5V_ALW +3.3V_ALW +3.3V_ALW_DSW +3.3V_ALW_PCH +RTC_CELL +1.8V_PRIM +1.0V_PRIM +1.0V_PRIM_CORE +5V_ALW2 +3.3V_ALW2 +3.3V_RTC_LDO +1.0V_MPHYGT | +3.3V_SUS +1.2V_MEM +1.0V_VCCST +2.5V_MEM | +5V_RUN +3.3V_RUN +0.6V_DDR_VTT +1.2V_RUN +VCC_CORE +VCC_GT +1.0VS_VCCIO +VCC_SA +1.8V_RUN |
|------------------------|---|--|--|
| S0 | ON | ON | ON |
| S3 | ON | ON | OFF |
| S5 S4/AC | ON | OFF | OFF |
| S5 S4/AC doesn't exist | OFF | OFF | OFF |

| Layer No. | Name | Er | Material | Thickness (Material SPEC.) Unit : mil | Thickness (Actuality) Unit : mil |
|---------------------------------|----------|-----|-------------|---|--|
| | | | SolderMask | IT-158 | 0.50 |
| | | | Add Plating | | 0.95 |
| 1 | Top | | Copper foil | 0.5oz | 0.65 |
| | | 3.7 | Prepreg | 1080 | 2.60 |
| 2 | GND1 | | Copper foil | 1oz | 1.35 |
| | | 3.7 | Core | 4mil | 4.00 |
| 3 | Sig 1 | | Copper foil | 1oz | 1.35 |
| | | 3.6 | Prepreg | 2116HRCx2 | 5.90 |
| 4 | GND1/PWR | | Copper foil | 1oz | 1.35 |
| | | 3.7 | Core | 4mil | 4.00 |
| 5 | Sig2 | | Copper foil | 1oz | 1.35 |
| | | 3.6 | Prepreg | 2116HRCx2 | 5.20 |
| 6 | Sig3 | | Copper foil | 1oz | 1.35 |
| | | 3.6 | Core | 4mil | 4.00 |
| 7 | GND2 | | Copper foil | 1oz | 1.35 |
| | | 3.7 | Prepreg | 1080 | 2.60 |
| 8 | Bottom | | Copper foil | 0.5oz | 0.65 |
| | | | Add Plating | | 0.95 |
| | | | SolderMask | | 0.50 |
| Overall Thickness (1.2mm ± 10%) | | | | 47.2 | 46.60000 1.18364 |



| USB3.0 | SSIC | PCIE | SATA | DESTINATION |
|-----------|--------|---------|---------|--|
| USB3.0-1 | | | | JUSB3-->Rear |
| USB3.0-2 | SSIC-1 | | | JNGFF2-->M2 3042(LTE) |
| USB3.0-3 | SSIC-2 | | | JUSB1-->Right |
| USB3.0-4 | | | | JUSB2-->Left |
| USB3.0-5 | | | | NA |
| USB3.0-6 | | | | NA |
| USB3.0-7 | | PCIE-1 | | JNGFF1-->M.2 3030(WIGIG) |
| USB3.0-8 | | PCIE-2 | | JNGFF1-->M.2 3030(WLAN) |
| USB3.0-9 | | PCIE-3 | | Card Reader |
| USB3.0-10 | | PCIE-4 | | LOM |
| | | PCIE-5 | | NA |
| | | PCIE-6 | | |
| | | PCIE-7 | | |
| | | PCIE-8 | | |
| | | PCIE-9 | SATA-0A | M.2 Socket 3 (Key M) M.2 2280 SSD (PCIex4 or SATA) |
| | | PCIE-10 | SATA-1A | |
| | | PCIE-11 | | |
| | | PCIE-12 | | |
| | | PCIE-13 | SATA-0B | NA |
| | | PCIE-14 | SATA-1B | NA |
| | | PCIE-15 | SATA-2 | JSATA1-->HDD SATA |
| | | PCIE-16 | SATA-3 | NA |
| | | PCIE-17 | SATA-4 | M.2 3042 (HCA or QCA LTE) SSD Cache |
| | | PCIE-18 | SATA-5 | NA |
| | | PCIE-19 | | NA |
| | | PCIE-20 | | NA |

| USB PORT# | DESTINATION |
|-----------|------------------------|
| 1 | JUSB3-->Rear |
| 2 | JUSB1-->Right |
| 3 | JUSB2 -->Left |
| 4 | Type C |
| 5 | NA |
| 6 | JNGFF2--> M.2 3030(BT) |
| 7 | NA |
| 8 | JNGFF2-->M2 3042(WWAN) |
| 9 | JEDP1-->Touch Screen |
| 10 | JUSH1-->USH |
| 11 | JEDP1-->Camera |
| 12 | NA |

| | | |
|-----|---|-----|
| USH | H | BIO |
|-----|---|-----|

| VIDEO | | DESTINATION |
|-------|---------|------------------|
| eDP | | LCD |
| DDI-B | | JHDMI1 |
| DDI-C | | Type-C |
| DDI-D | DeMux 1 | M.2 3030 (WiGig) |
| | | MB VGA |

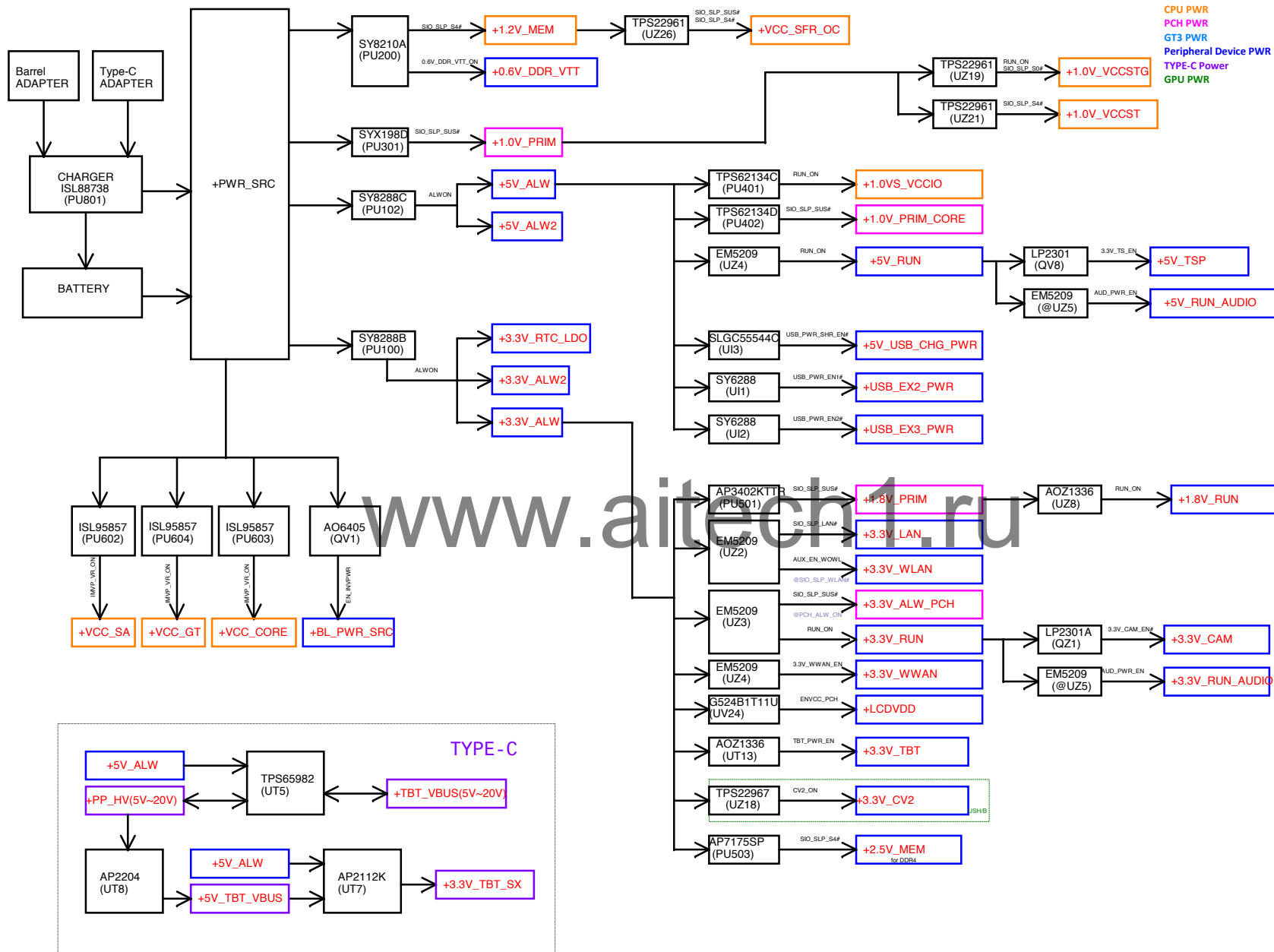
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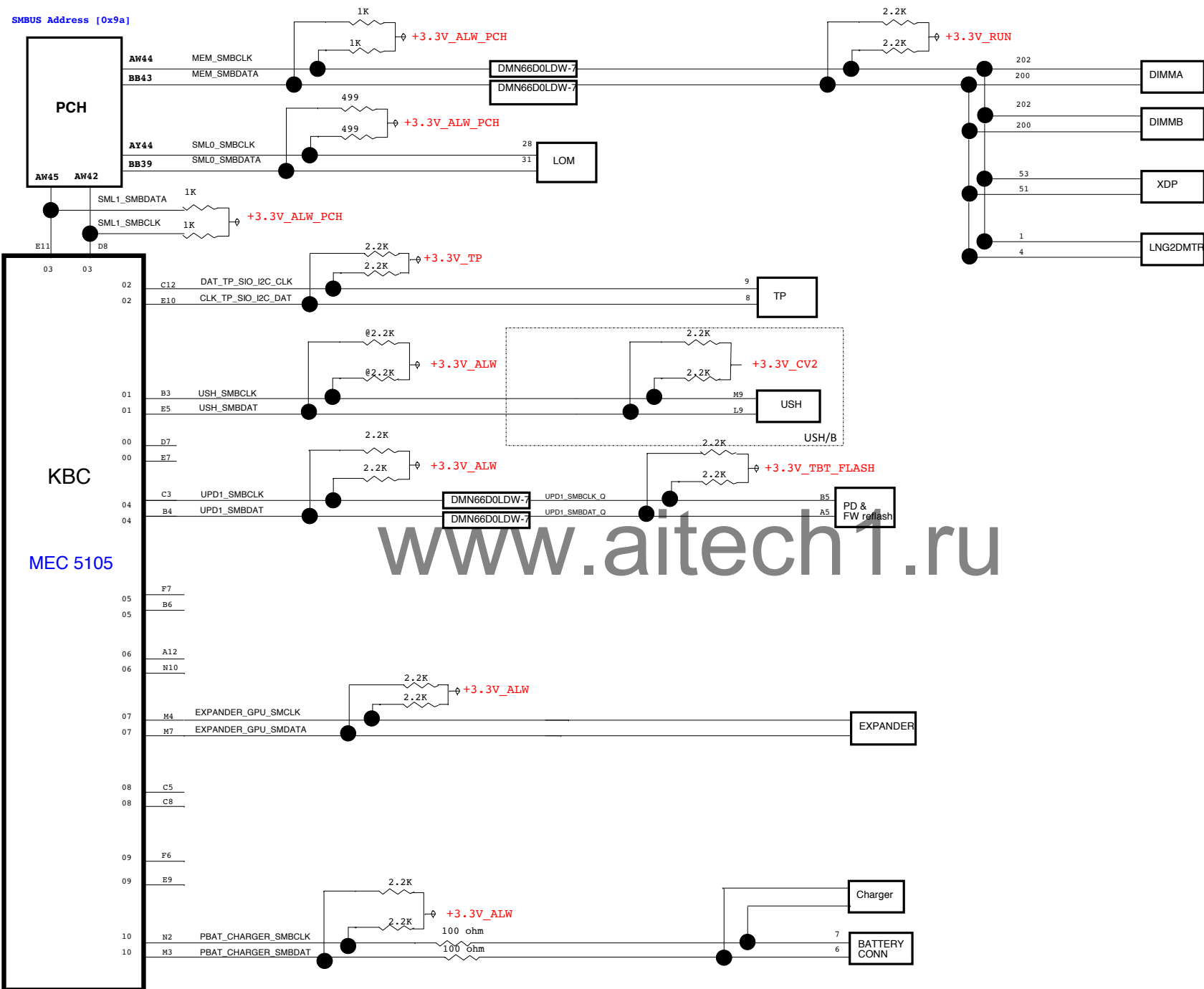
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Port Assignment

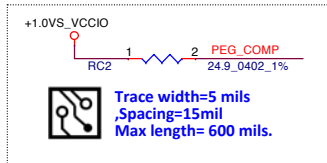
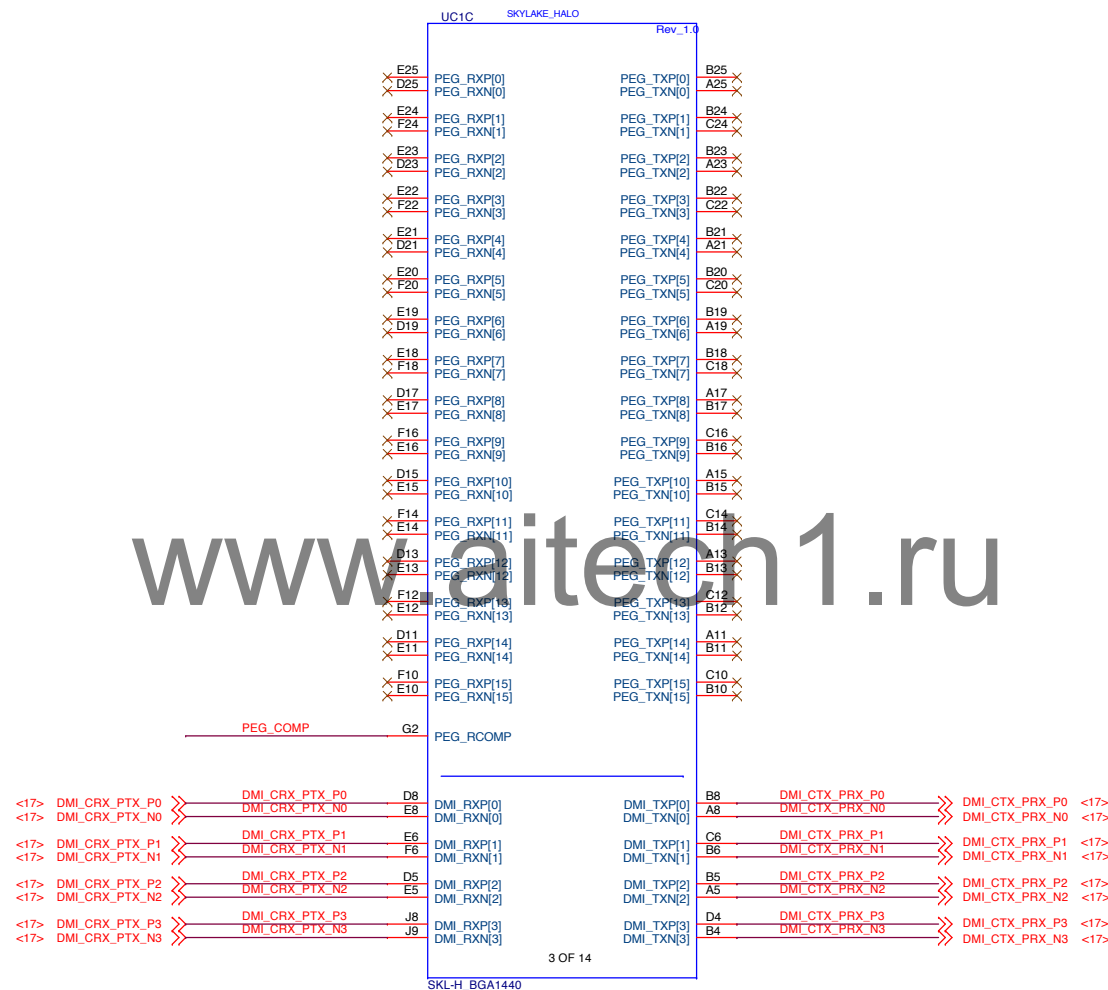
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| Size | Document Number | Rev 0.2 | |
| A | LA-E151P | | |
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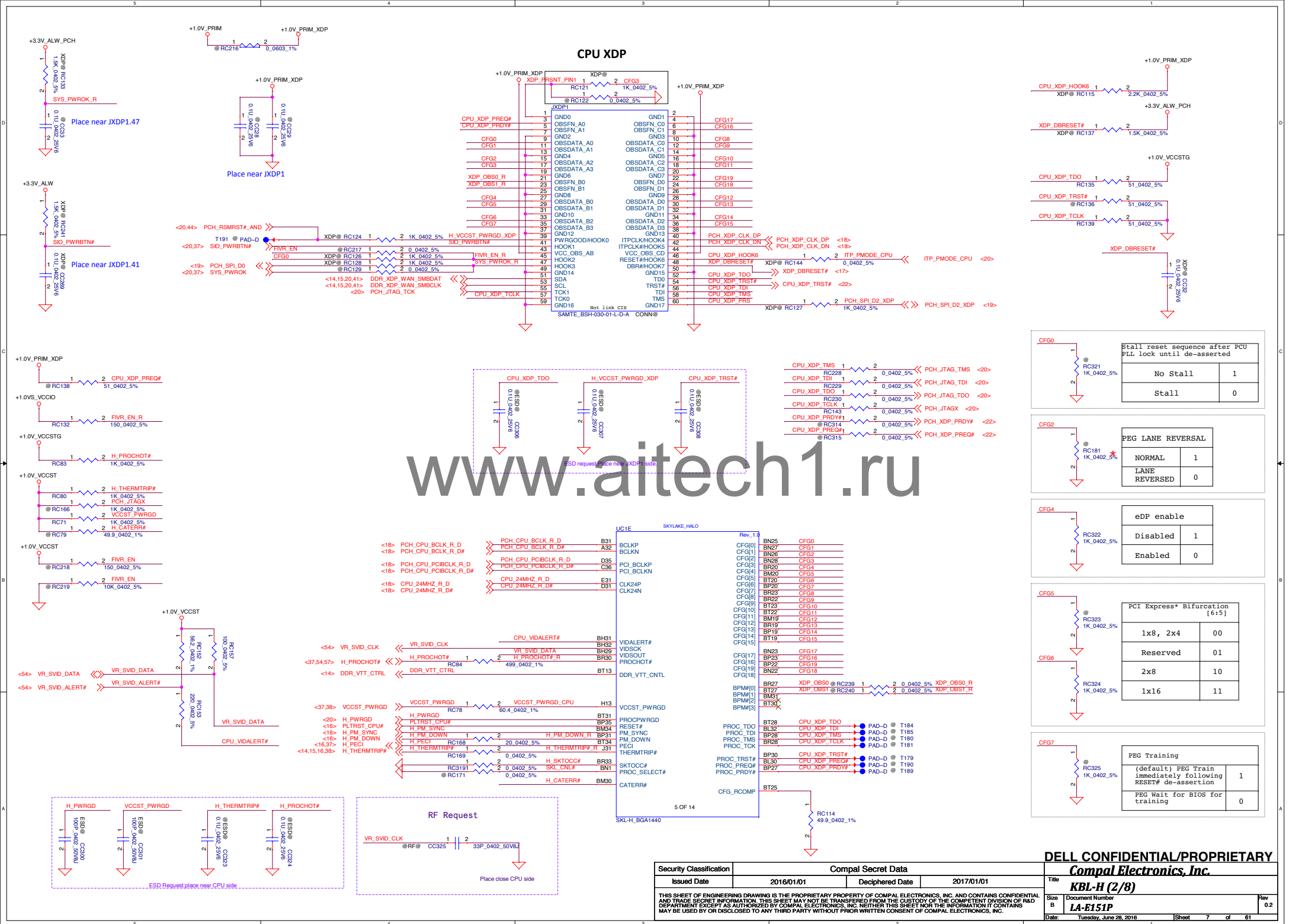


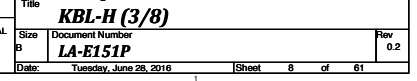


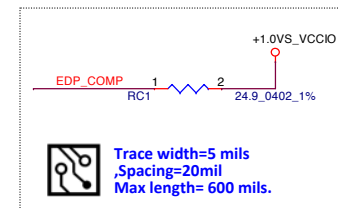
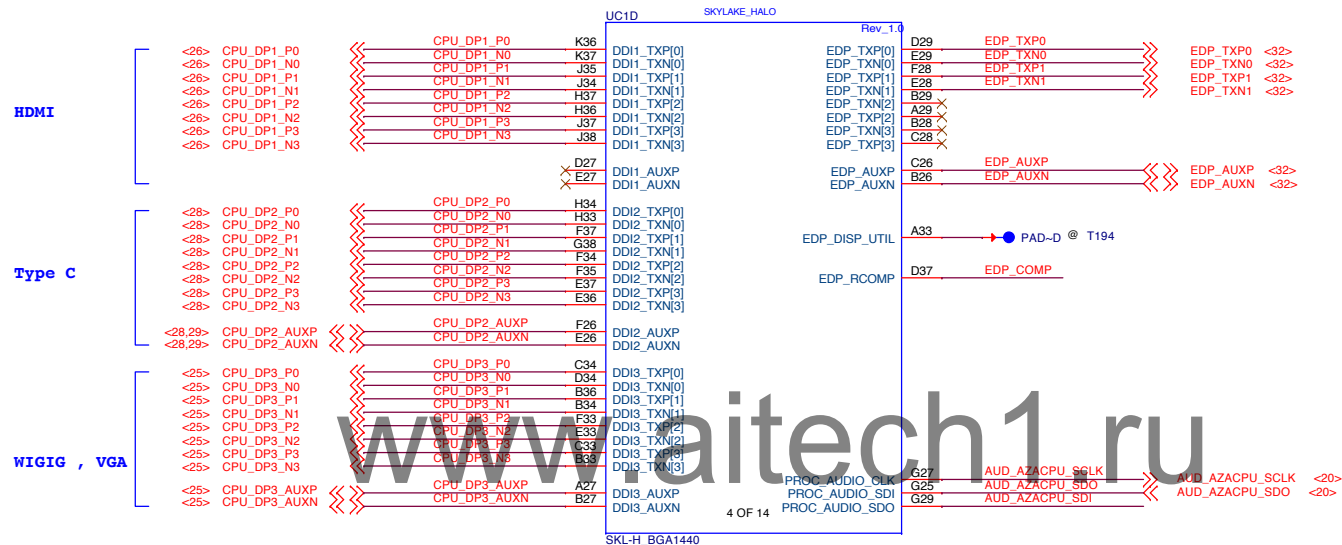
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| | | | | Document Number | |
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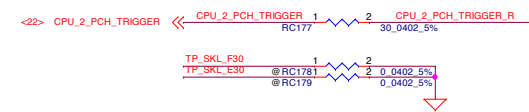
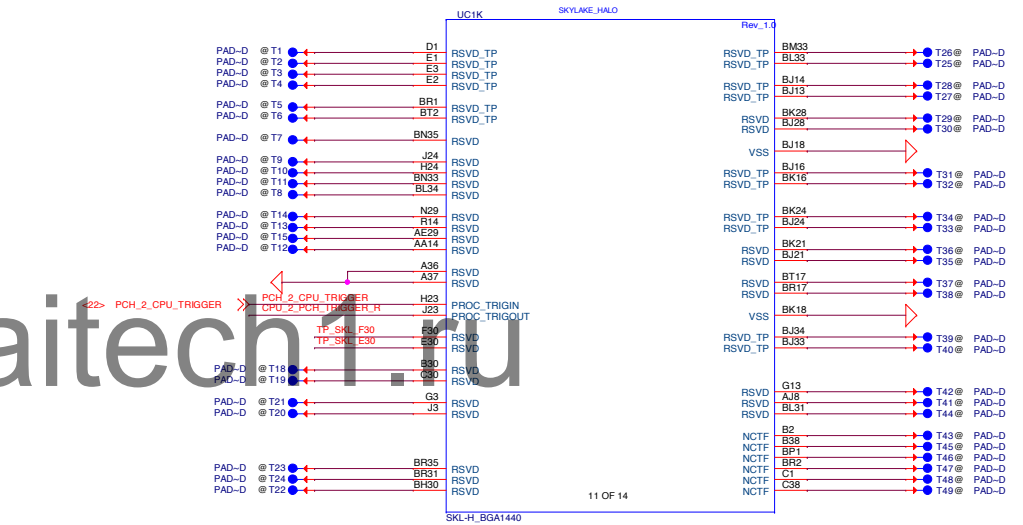
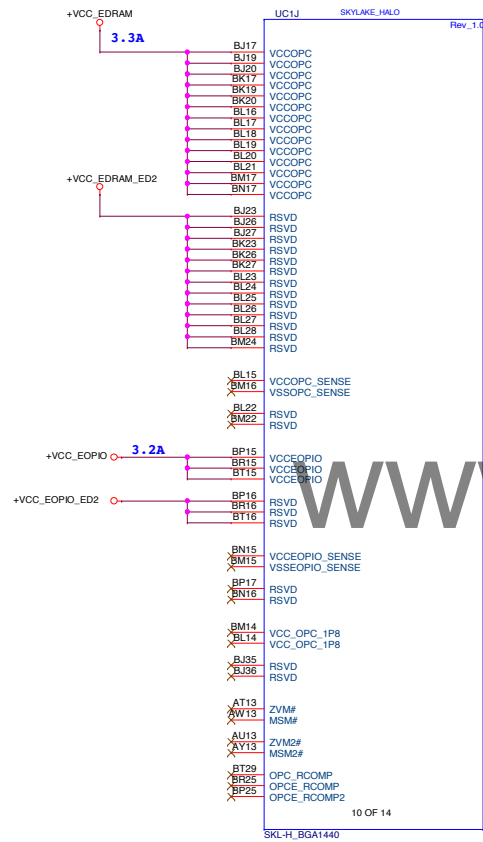
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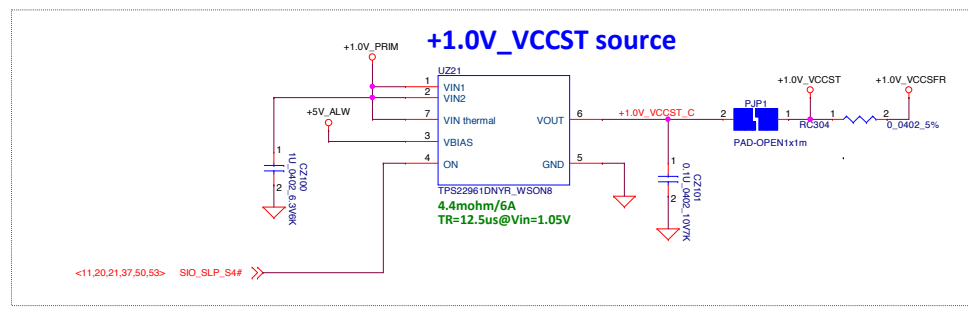
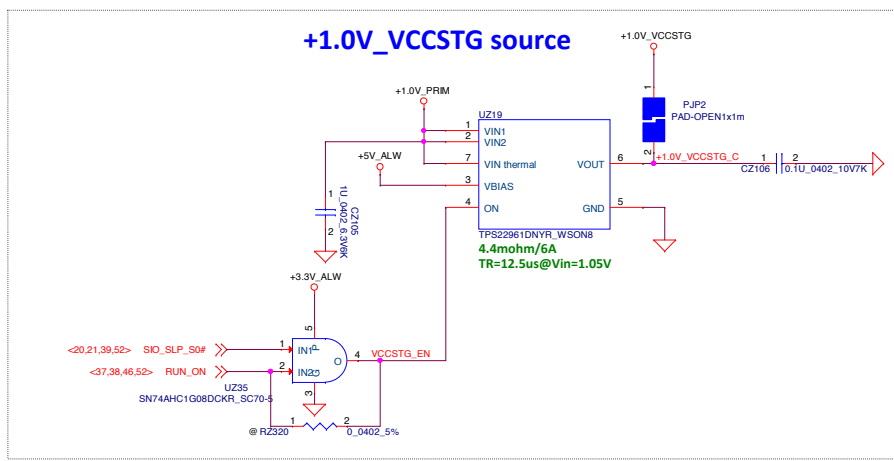
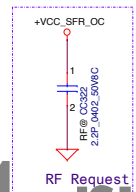
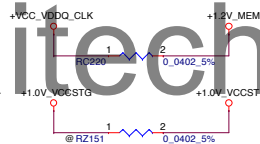
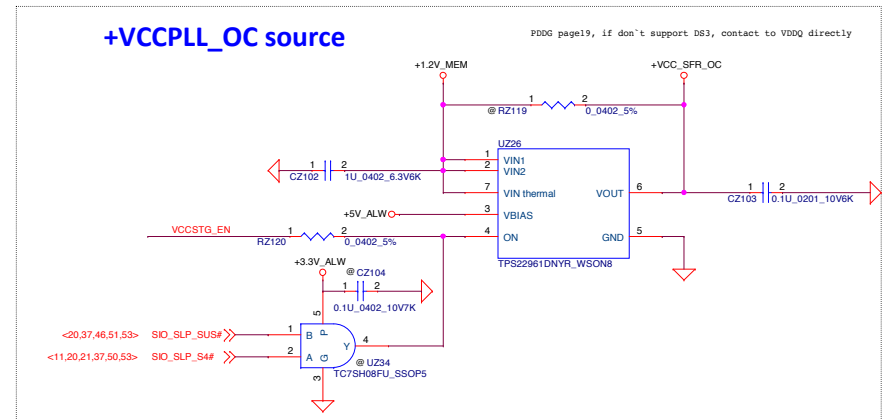
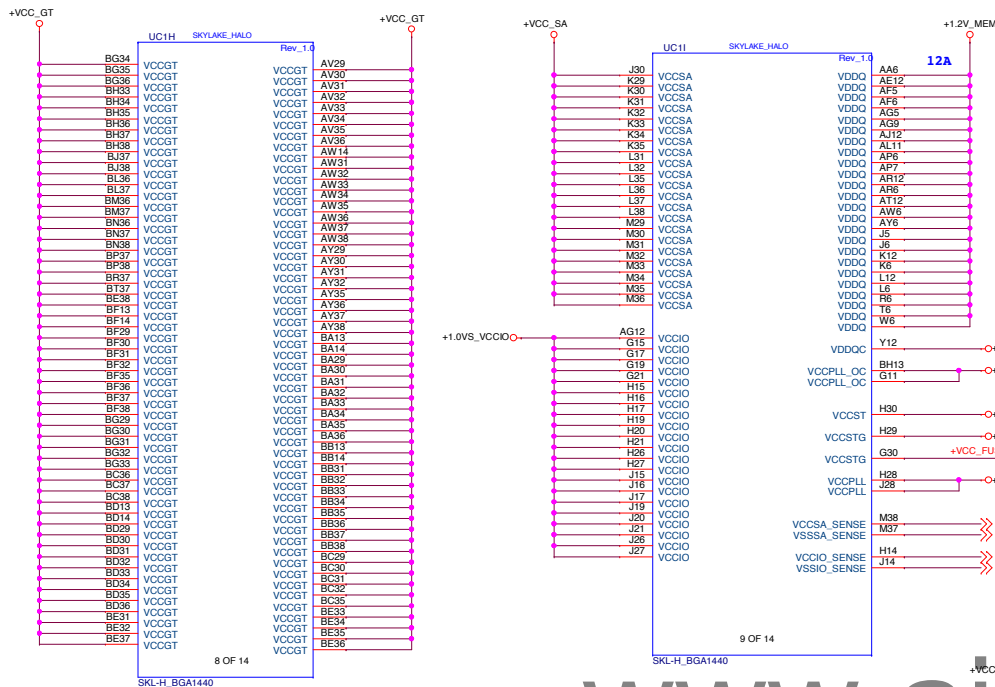






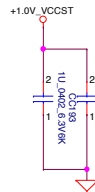
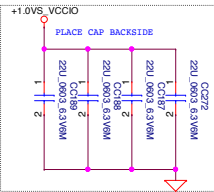
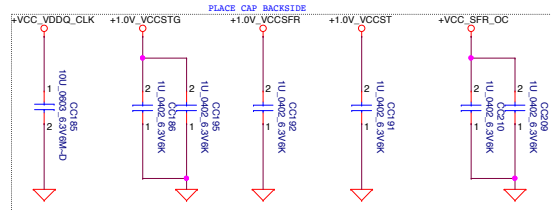
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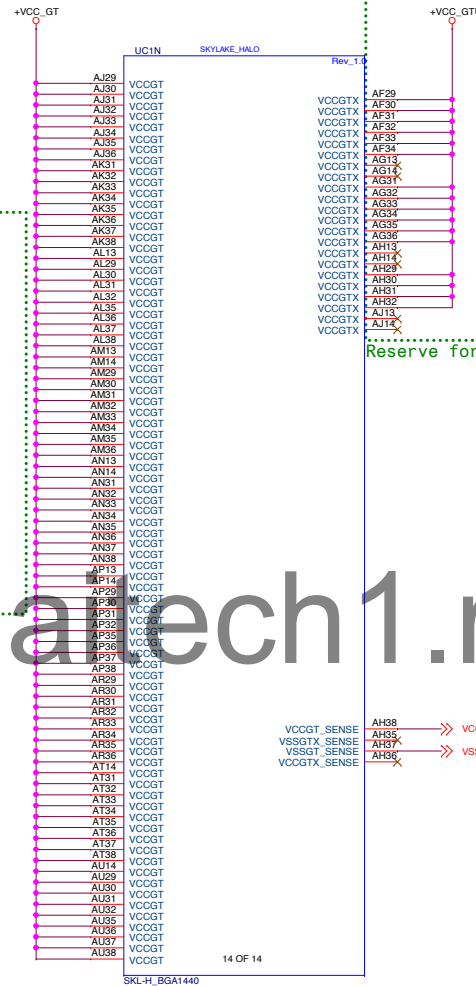
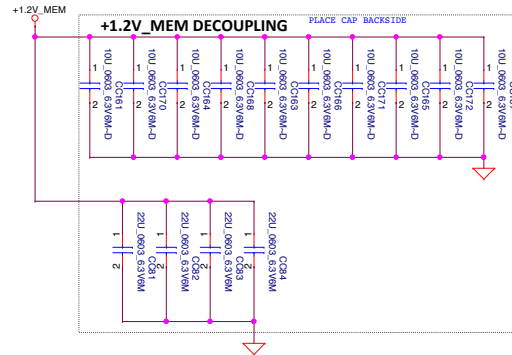


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For SKL-H 4+2
Remove VCCOPC/VCCEPIO/
VCCOPC_1P8 Cap



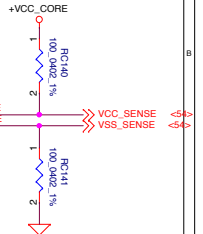
Remove to Power (+VCC_SA cap)



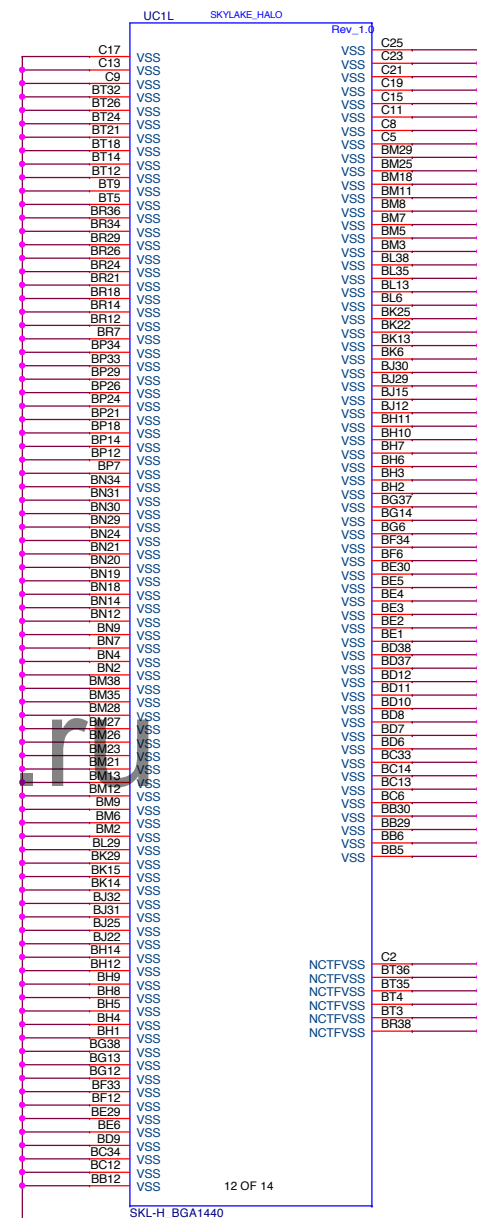
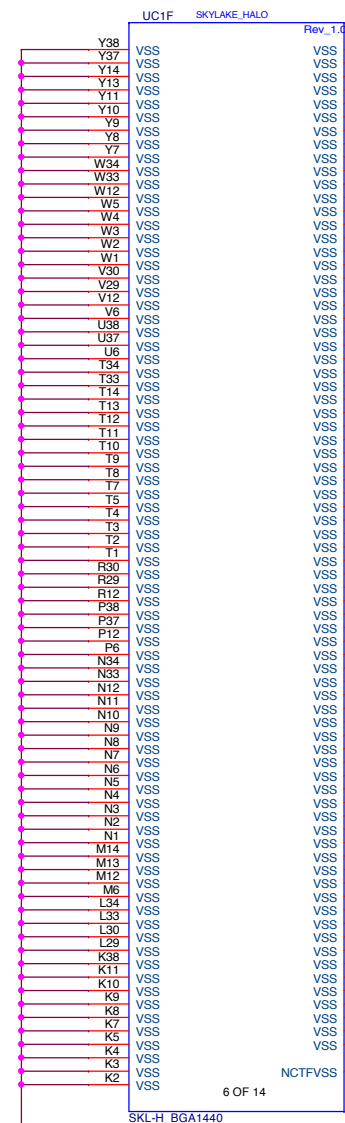
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VSSGTX_SENSE AH35 >>> VSS_GT_SENSE <54>
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VCCGTX_SENSE AH36 >>> VSS_GT_SENSE <54>

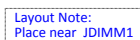


VSS_SENSE 1 2 49.9_0402_1%

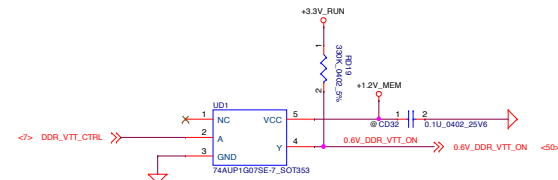
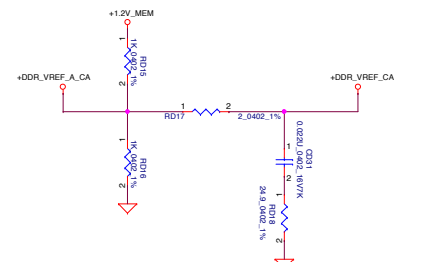
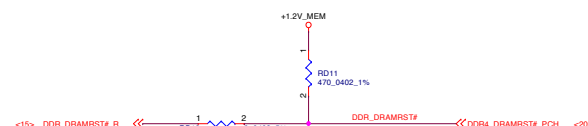


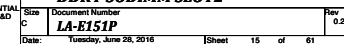
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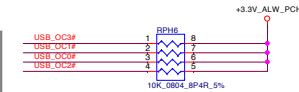


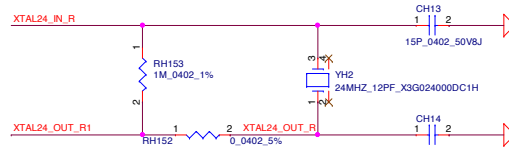
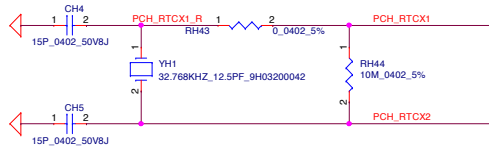
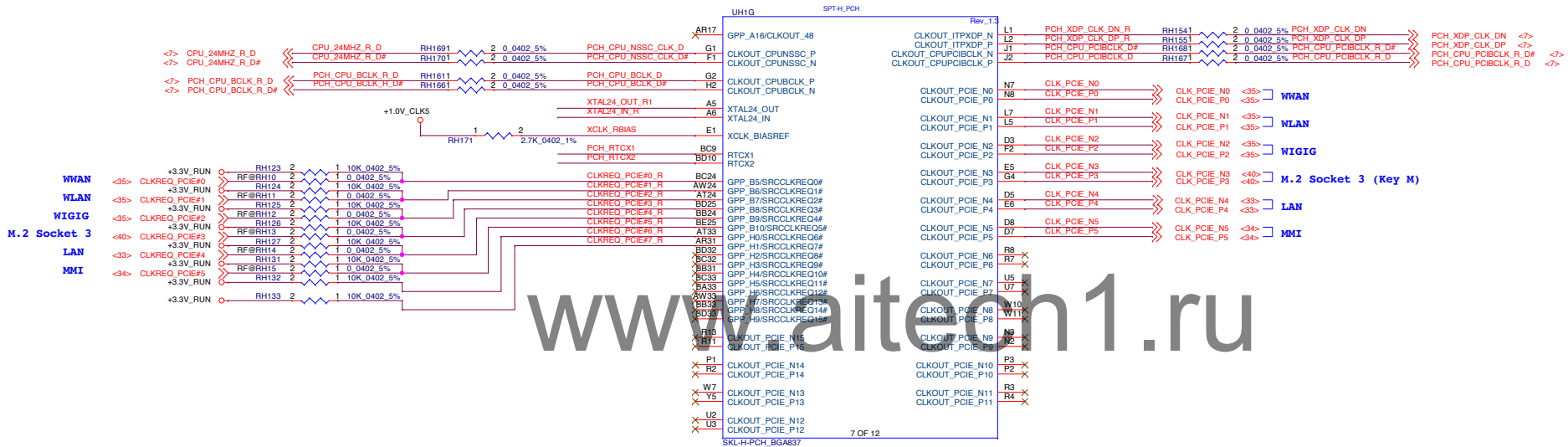


| | | |
|----------------|-----------|-------------|
| Byte[0] | DQ[7:0] | DQS/DQS#[0] |
| Byte[1] | DQ[15:8] | DQS/DQS#[1] |
| Byte[2] | DQ[23:16] | DQS/DQS#[2] |
| Byte[3] | DQ[31:24] | DQS/DQS#[3] |
| Byte[4] | DQ[39:32] | DQS/DQS#[4] |
| Byte[5] | DQ[47:40] | DQS/DQS#[5] |
| Byte[6] | DQ[55:48] | DQS/DQS#[6] |
| Byte[7] | DQ[63:56] | DQS/DQS#[7] |

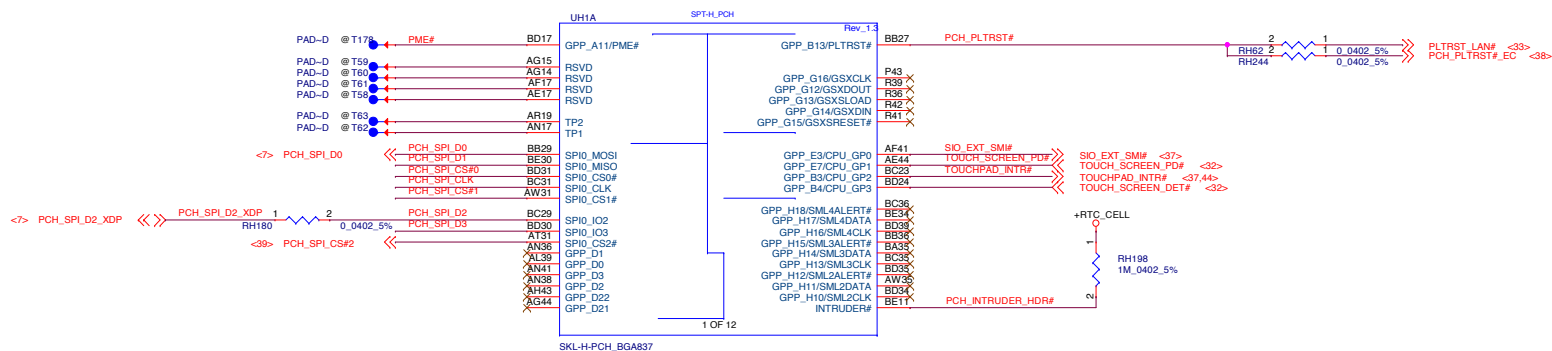
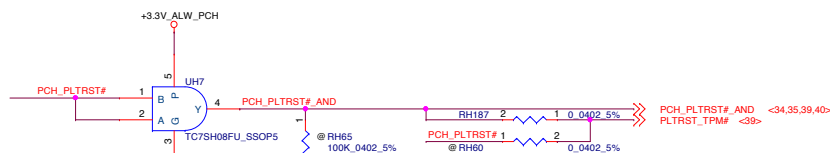






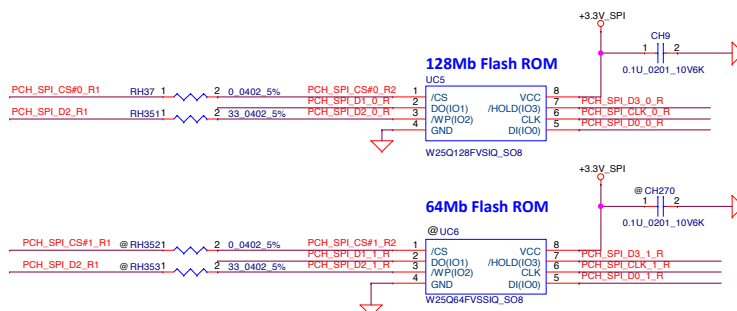
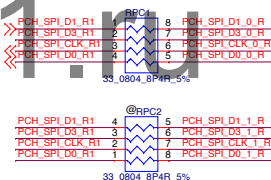
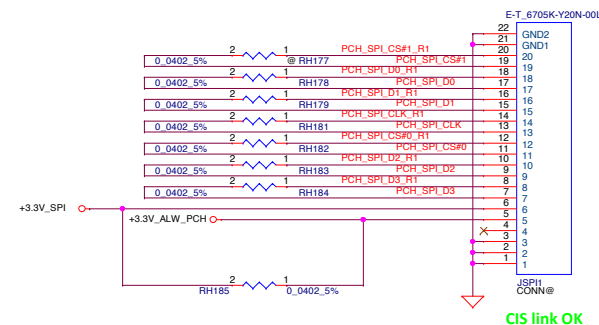
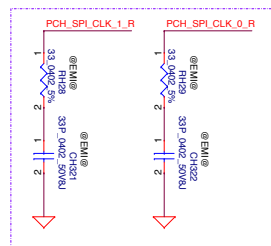


| Security Classification | | | | Compal Secret Data | | DELL CONFIDENTIAL/PROPRIETARY | |
|---|--|--|--|--------------------|--|-------------------------------|--|
| Issued Date | | | | 2016/01/01 | | Deciphered Date | |
| 2017/01/01 | | | | 2017/01/01 | | 2017/01/01 | |
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| Size B | | | | Document Number | | LA-E151P | |
| Date: Thursday, June 30, 2016 | | | | Sheet | | 18 of 61 | |

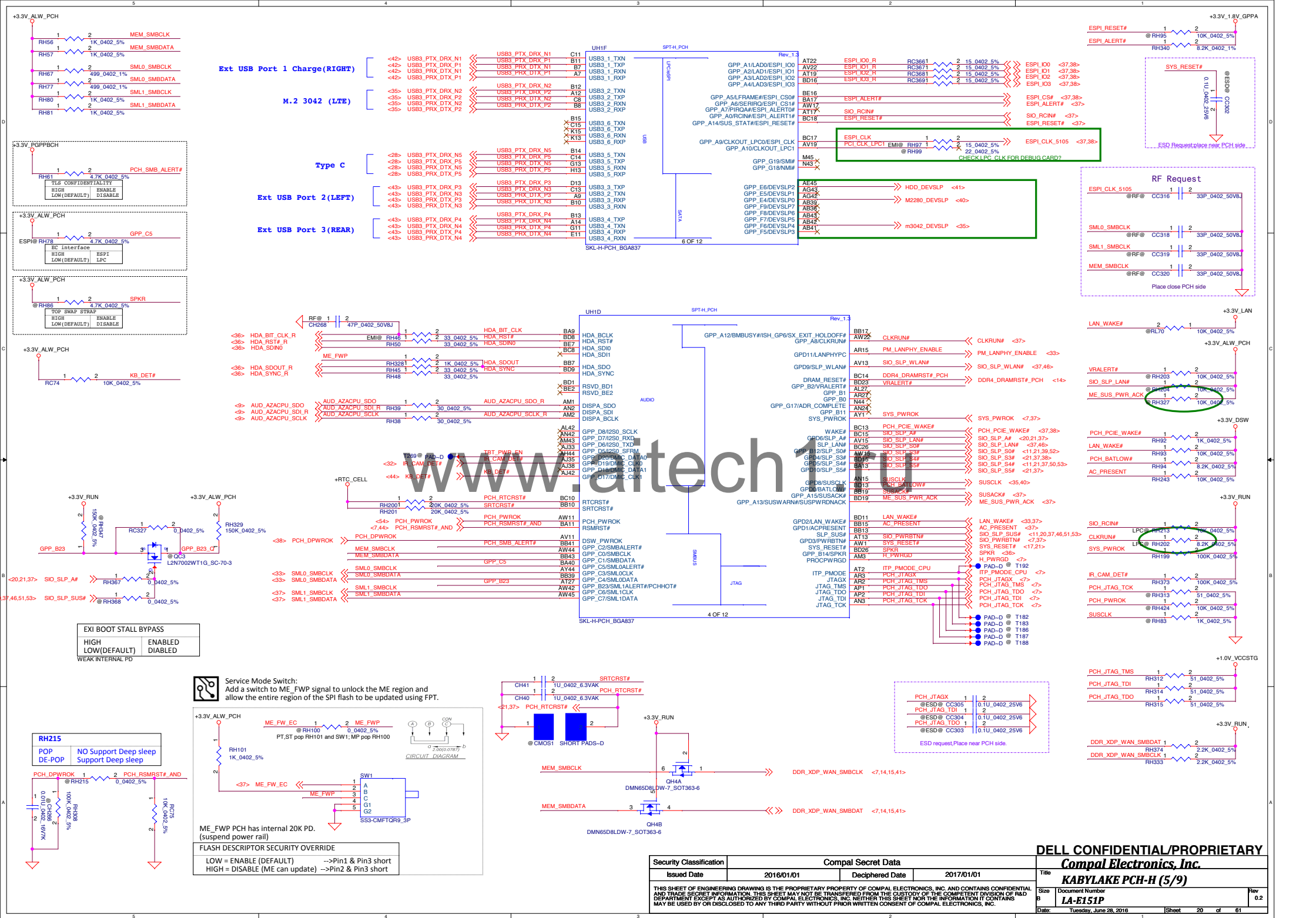


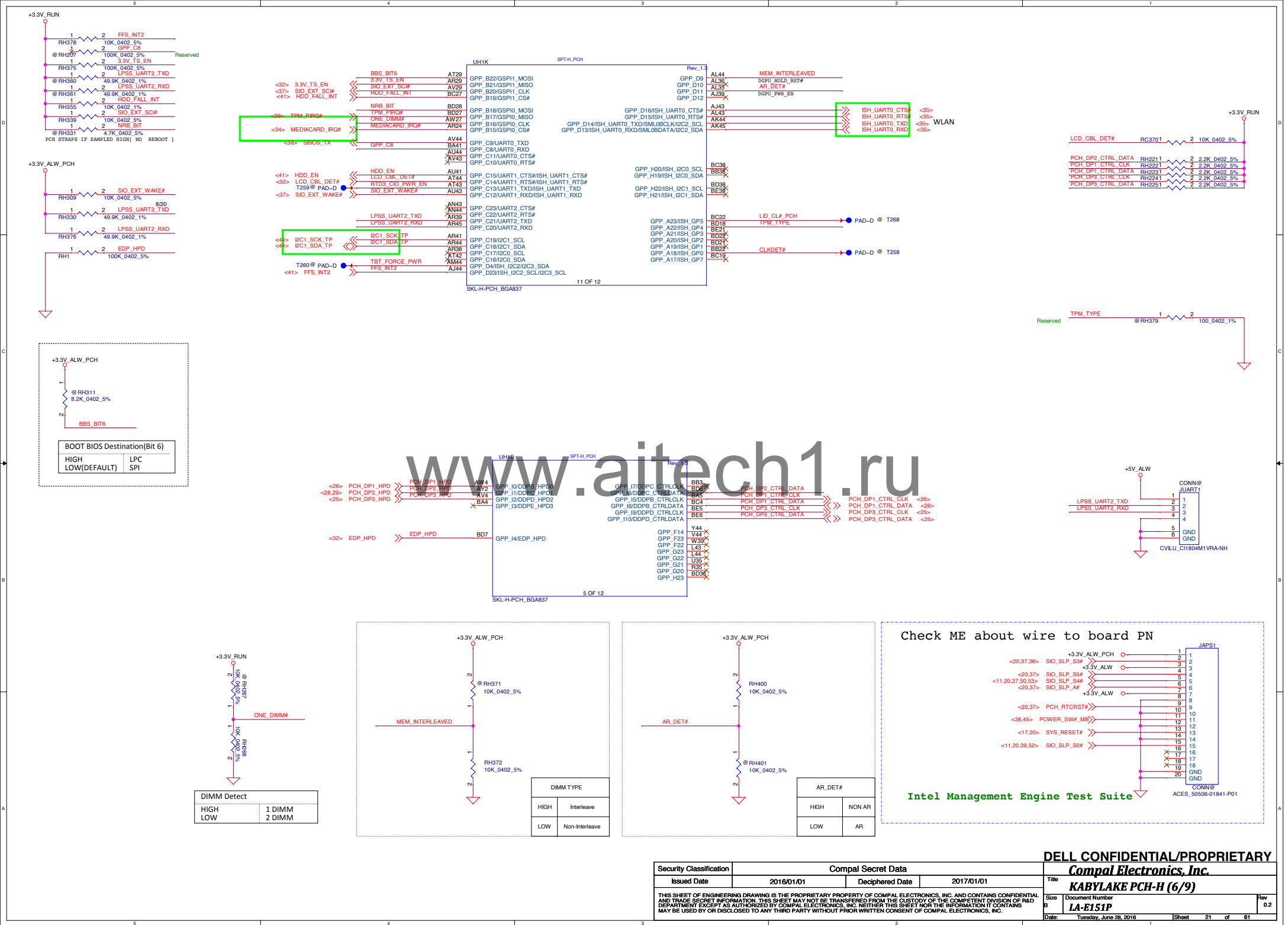
Option 1: Implement a 1 kOhm pull-down resistor on the signal and de-populate the required 1 kOhm pull-up resistor. In this case, customers must ensure that the SPI flash device on the platform has HOLD functionality disabled by default.

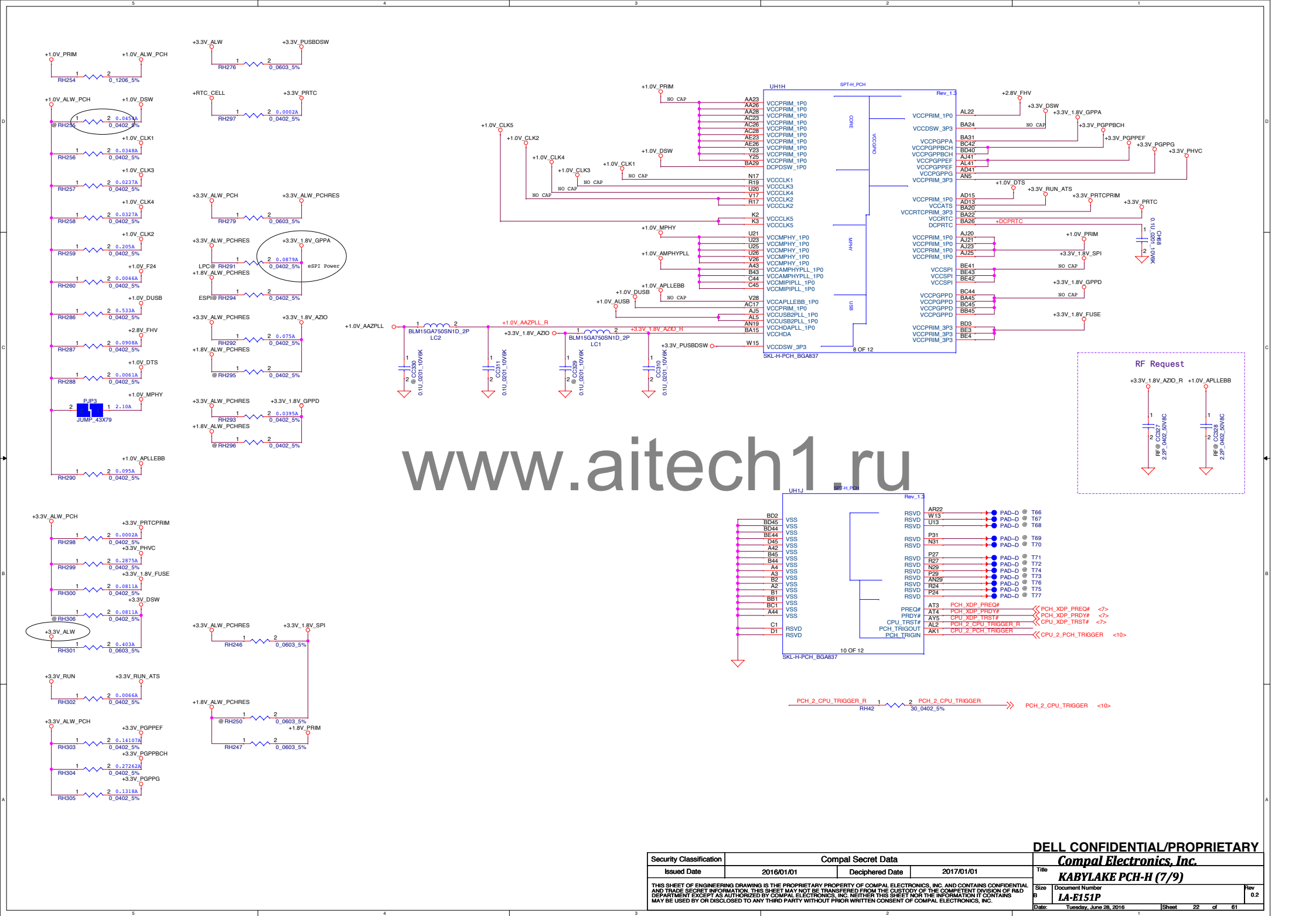
Note that the pull down resistor on SPI0_IO3 is only needed for SKL U/Y platforms with FS and SKL S/H platforms with pre-FS1/FS1 samples.

Need check

| | | | | | |
|---|------------|---------------------------|------------|--|---------------------------------|
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| | | | | Size | Document Number |
| | | | | LA-E151P | |
| | | | | Date: | Tuesday, June 28, 2016 |
| | | | | Sheet | 19 of 61 |



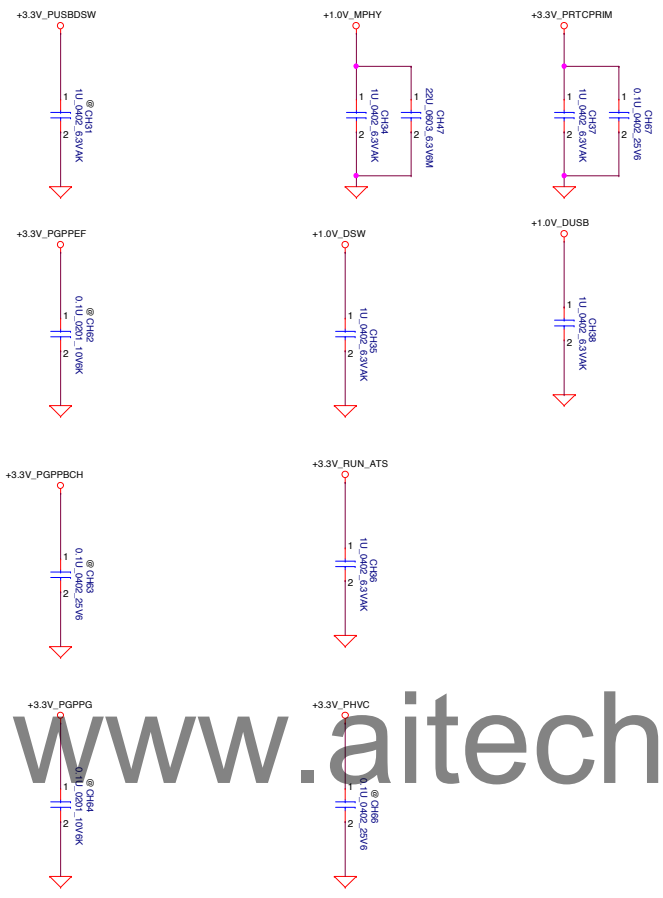
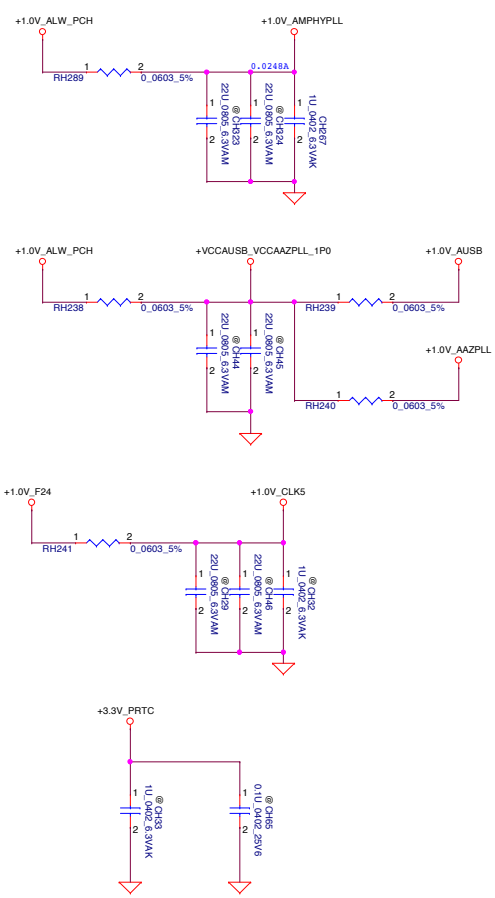




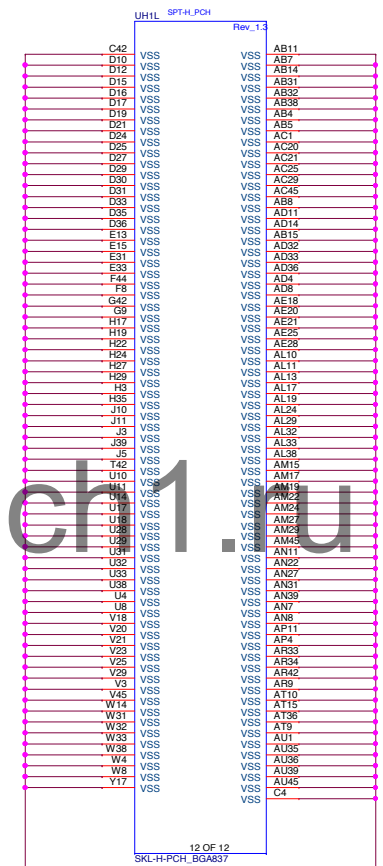
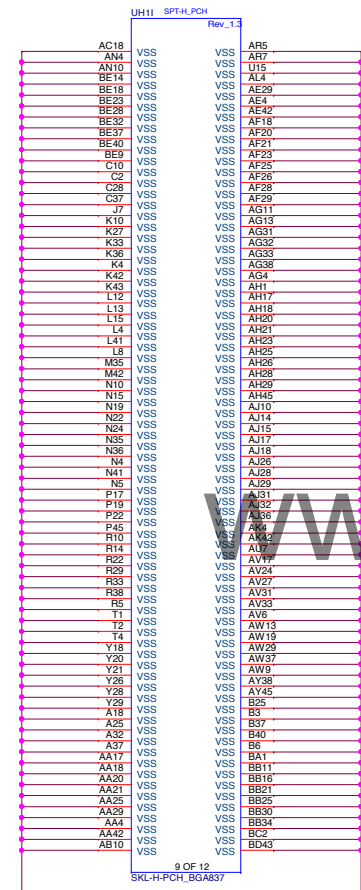
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| | | | | | |
|---|--|----------------------|--|-------------------------------|--|
| Security Classification | | Compal Secret Data | | DELL CONFIDENTIAL/PROPRIETARY | |
| Issued Date | | 2016/01/01 | | Document Number | |
| Deciphered Date | | 2017/01/01 | | LA-E151P | |
| Title | | KABYLAKE PCH-H (7/9) | | Rev | |
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| Sheet | | 22 | | of | |
| 61 | | Rev | | 0.2 | |

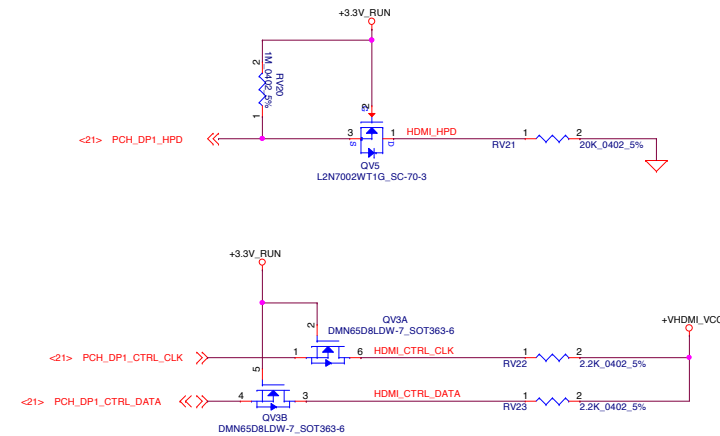
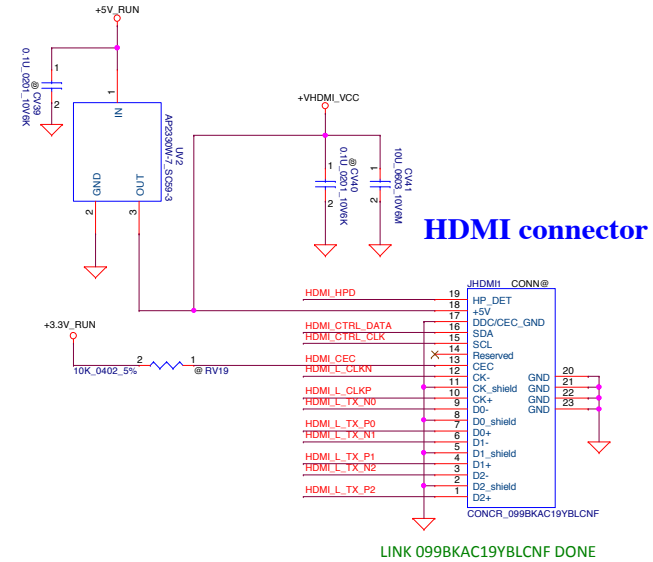
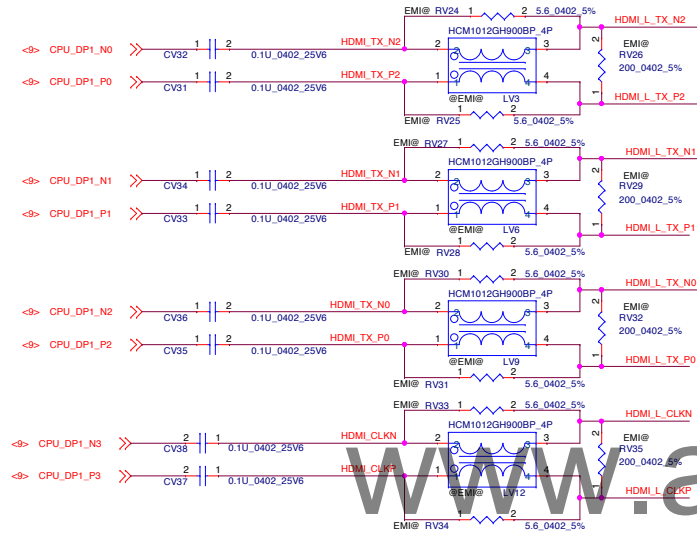
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| | | | | | | | | | | | |
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| Security Classification | | Compal Secret Data | | DELL CONFIDENTIAL/PROPRIETARY | | | | | | | |
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| | | | | | | | | KABYLAKE PCH-H (8/9) | | | |
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| | | | | LA-E151P | | 0.2 | | | | | |
| | | | | Date: | | Tuesday, June 28, 2016 | | Sheet | | 23 of 61 | |
| | | | | | | | | | | | |



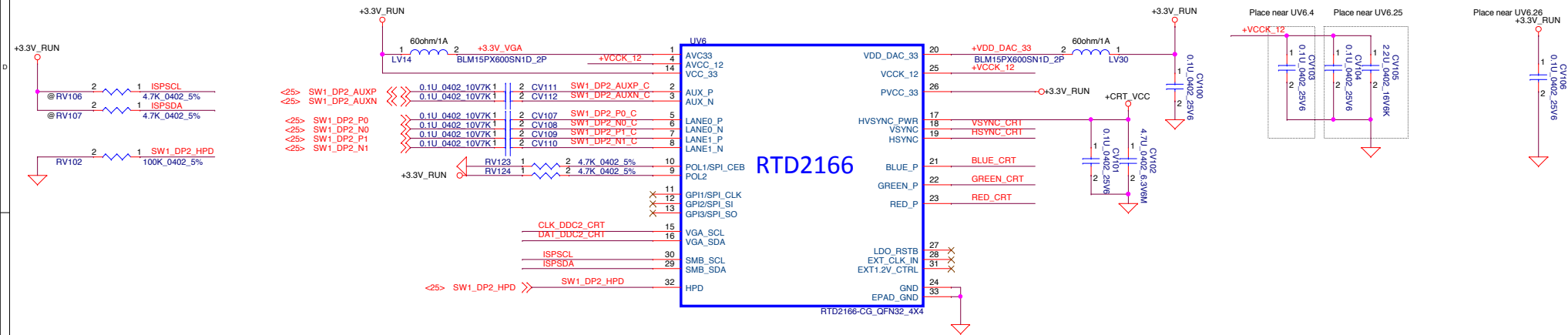




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| | | | | | | LA-E151P | 0.2 |
| | | | | | | Date: Tuesday, June 28, 2016 | Sheet 26 of 61 |

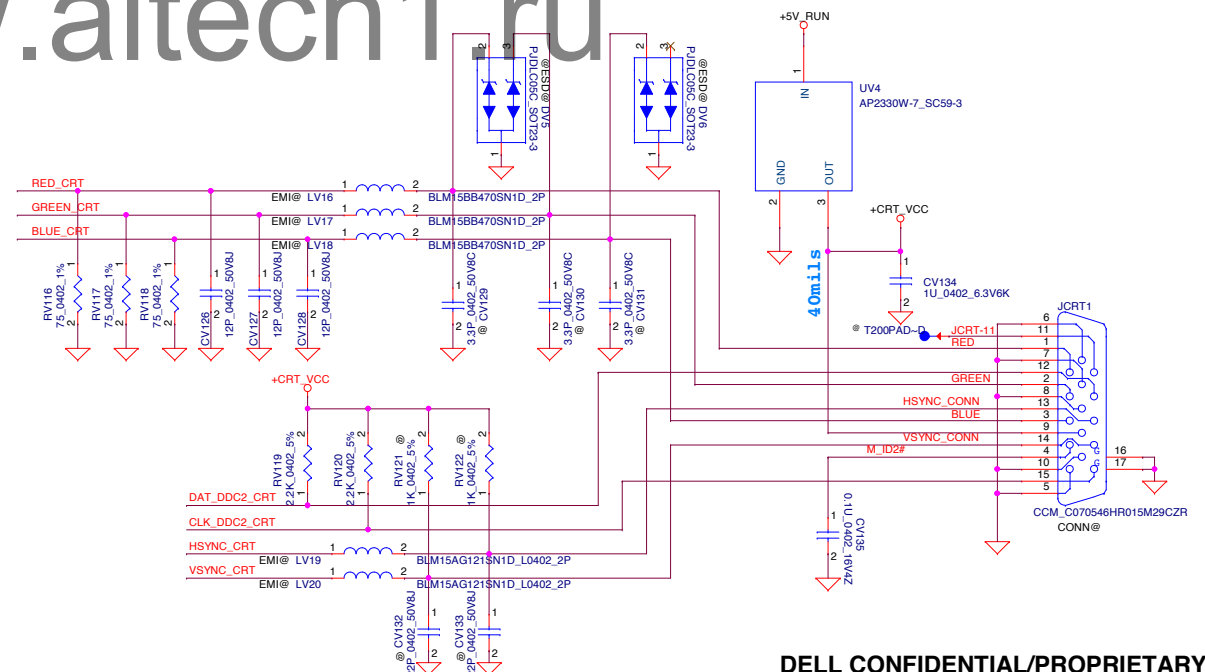
For TBT SW2_DP2
For non-TBT SW1_DP2

For Realtek Solution



| | | POL1(P10) | |
|--------------|---|-----------|--------|
| | | 0 | 1 |
| POL2 (P9) | 0 | X | X |
| | 1 | ROM | EEPROM |

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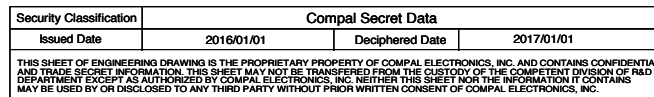
DP to VGA & VGA Conn

Document Number
LA-E151P

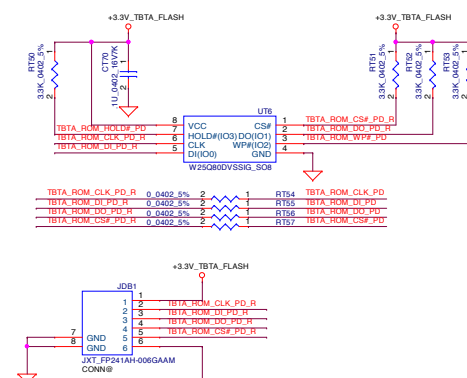
Rev
0.2

| | | | | | |
|-------|------------------------|-------|----|----|----|
| Date: | Tuesday, June 28, 2016 | Sheet | 27 | of | 61 |
|-------|------------------------|-------|----|----|----|

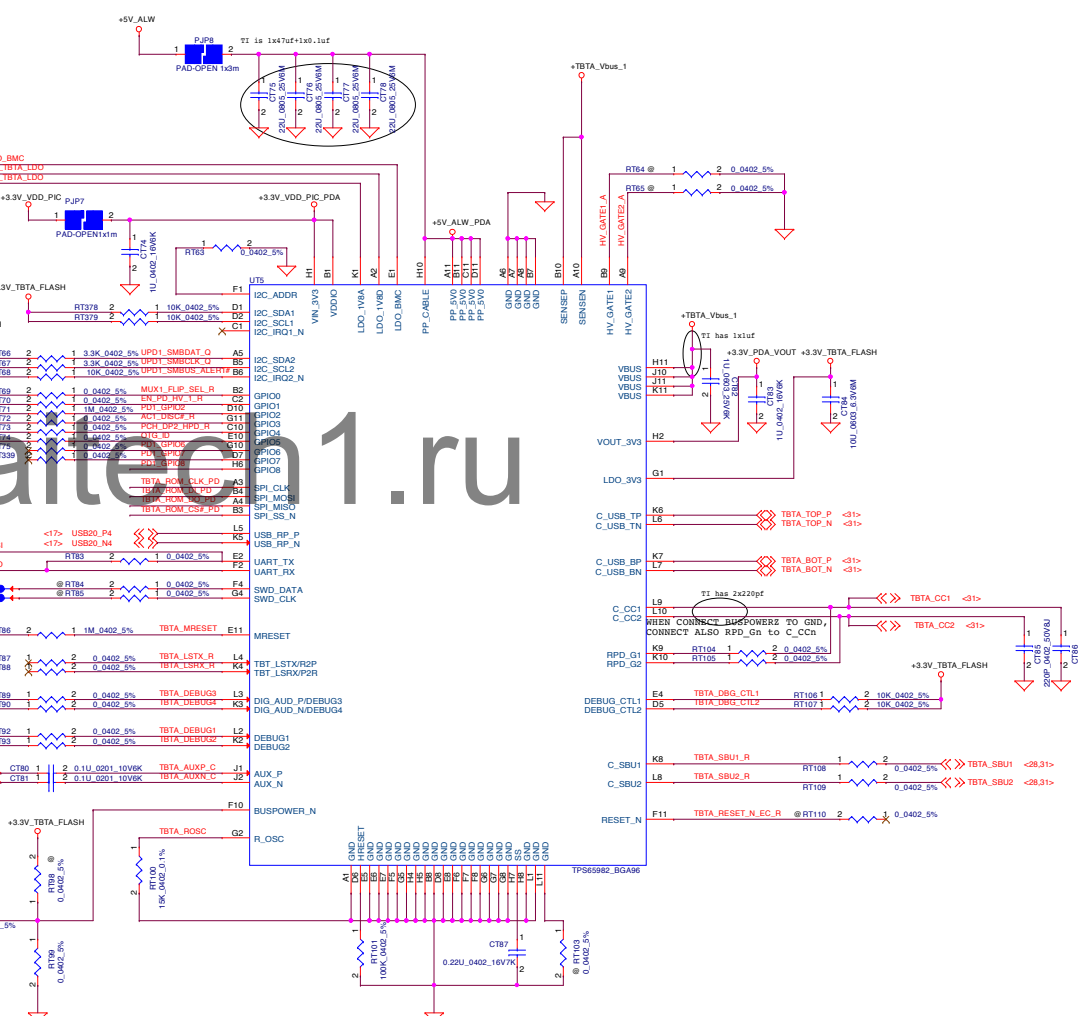
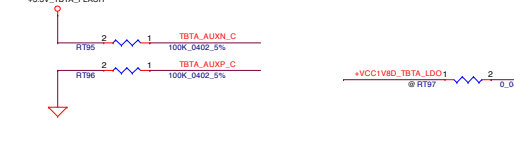
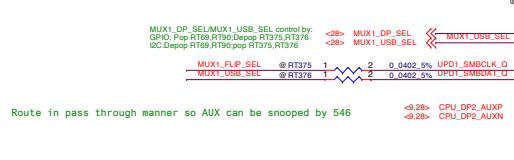
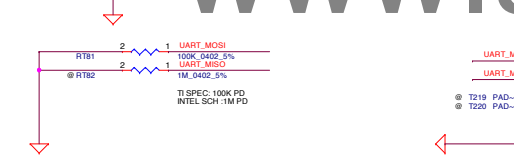
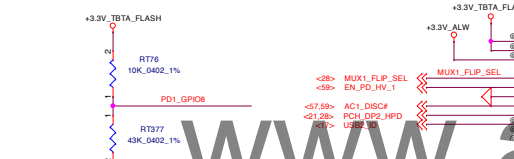
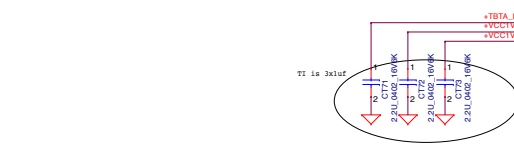
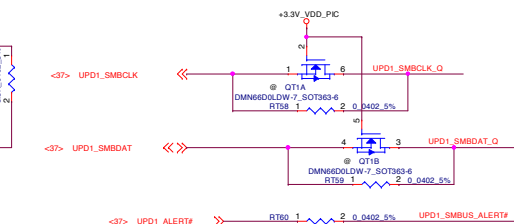
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| Issued Date | 2016/01/01 | Deciphered Date | 2017/01/01 |
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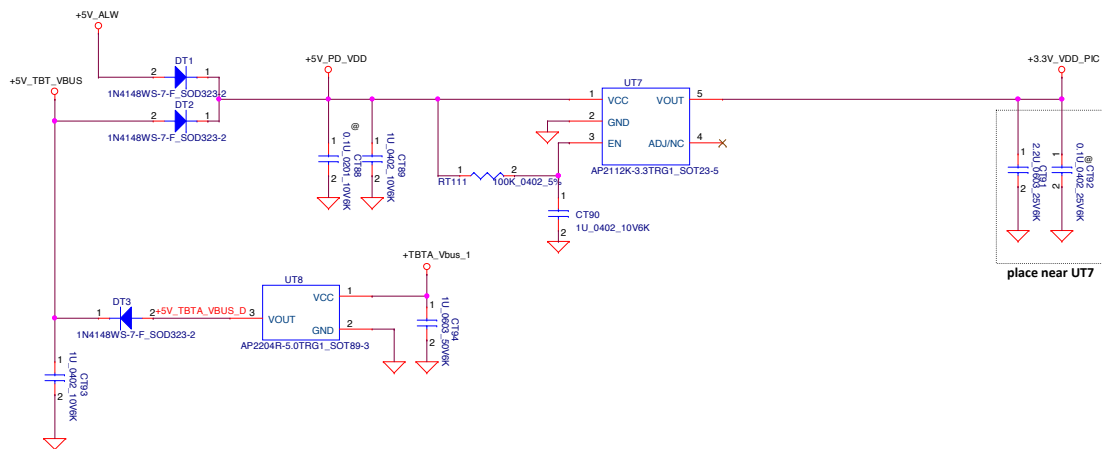
For Non-AR config



| DIV = R2 / (R1+R2) | | Factory Device Configuration | | Description | |
|--------------------|---------|------------------------------|--|--|--|
| DIV_min | DIV_max | | | | |
| 0.00 | 0.08 | 0 | | UFP only SV @0.9A Sink capability with "Ask for Max" for anything from 0.9 - 3.0A TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported | |
| 0.10 | 0.18 | 1 | | UFP only SV @0.9A Sink capability with "Ask for Max" for anything from 0.9 - 3.0A TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported | |
| 0.20 | 0.28 | 2 | | UFP only SV @0.9A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported | |
| 0.30 | 0.38 | 3 | | UFP only SV @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes - Sink, C and D pin configuration TI VID supported | |
| 0.40 | 0.48 | 4 | | DRP SV @0.9-3.0A Sink capability SV @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported Accepts data and power role swaps, but does not initiate | |
| 0.50 | 0.58 | 5 | | DRP SV @0.9-3.0A Sink capability SV @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes - Source, C, D, and E pin configurations TI VID supported Accepts power role swaps but will not initiate Accepts data role swaps, but does not initiate | |
| 0.60 | 0.68 | 6 | | DRP SV @0.9-3.0A Sink capability SV @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes - Source, C, D, and E pin configurations TI VID supported Accepts power role swaps but will not initiate Accepts data role swaps, but does not initiate | |
| 0.70 | 1.00 | 7 | | Infinite boot retry from Flash to Host UF cycles. | |



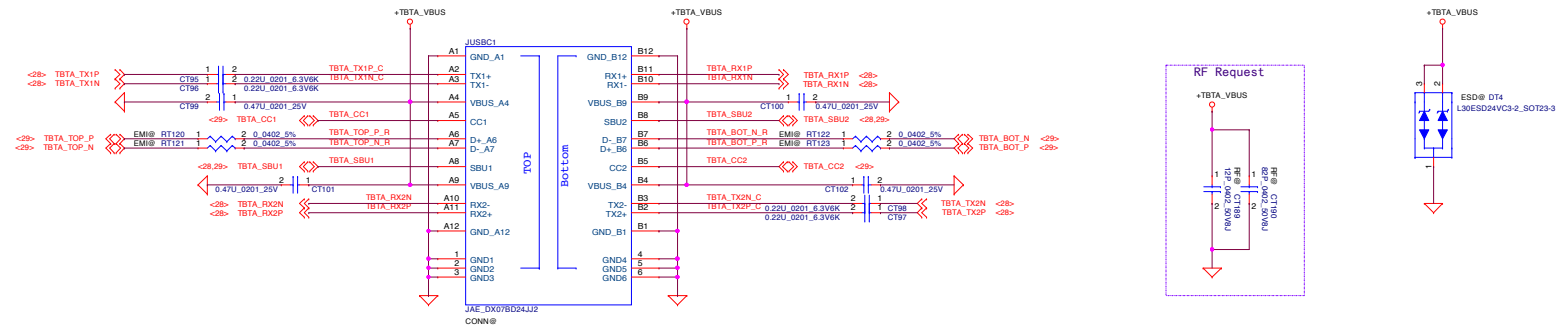
Need Link TPS65982D



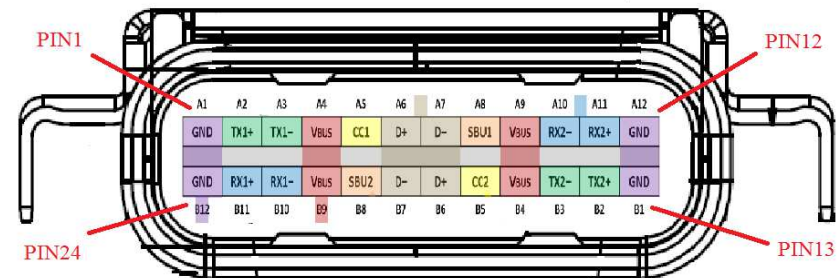
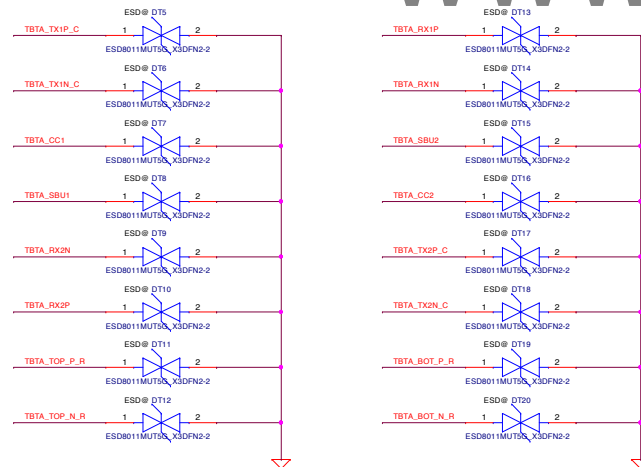
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|---|--|--------------------|--|-------------------------------|--|
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| 2016/01/01 | | 2017/01/01 | | [Type C]PD Power | |
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| Date: Tuesday, June 28, 2016 | | Sheet 30 of 61 | | Document Number LA-E151P | |

For NON AR Config

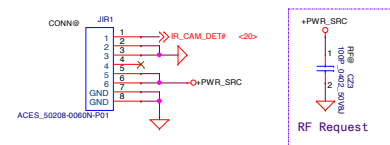
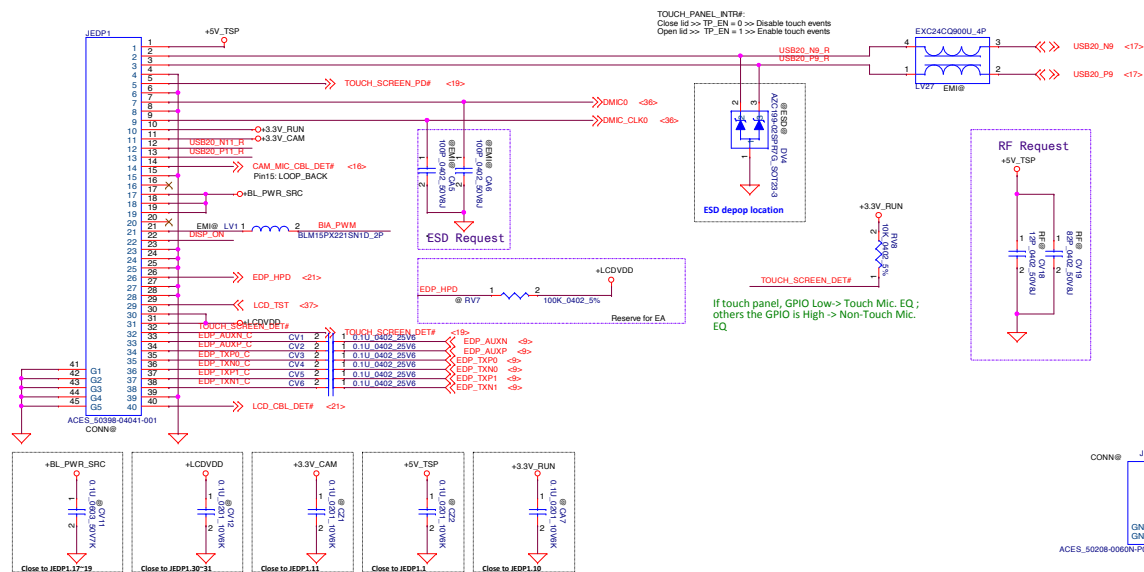


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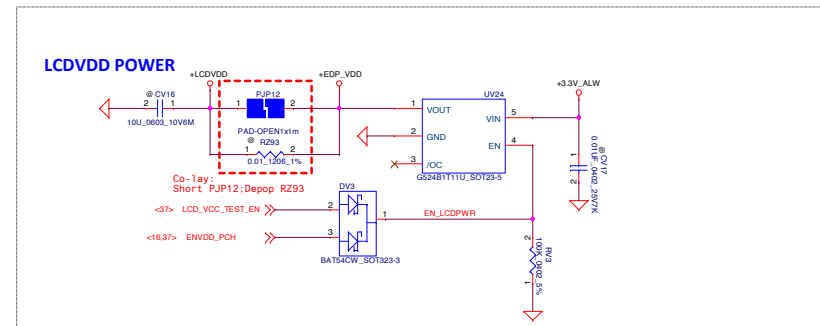
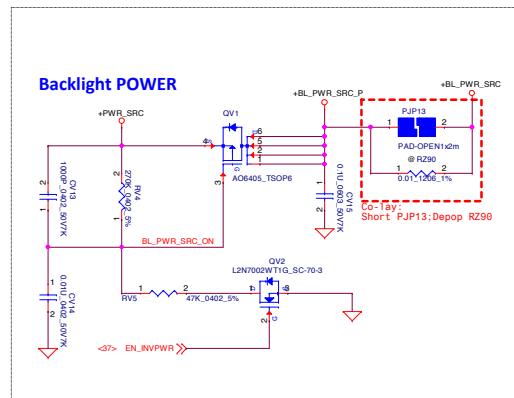
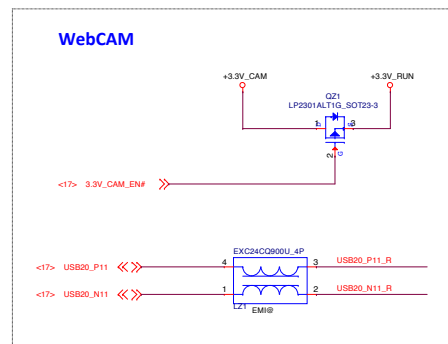
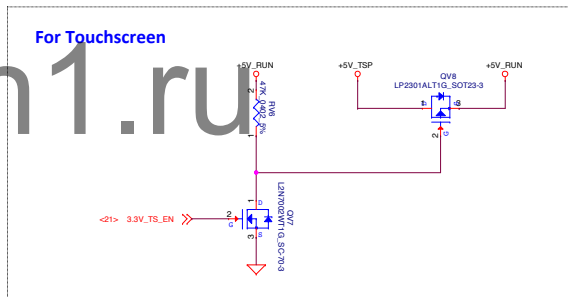
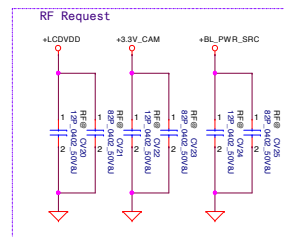


| | | | | | |
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| Security Classification | | Compal Secret Data | | DELL CONFIDENTIAL/PROPRIETARY | |
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| Size | Document Number | | | Rev | 0.2 |
| | LA-E151P | | | | |
| Date | Tuesday, June 28, 2016 | | | Sheet | 31 of 61 |

For Breckenridge 14



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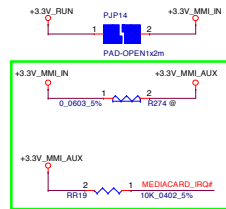
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

eDP CONN & Touch screen

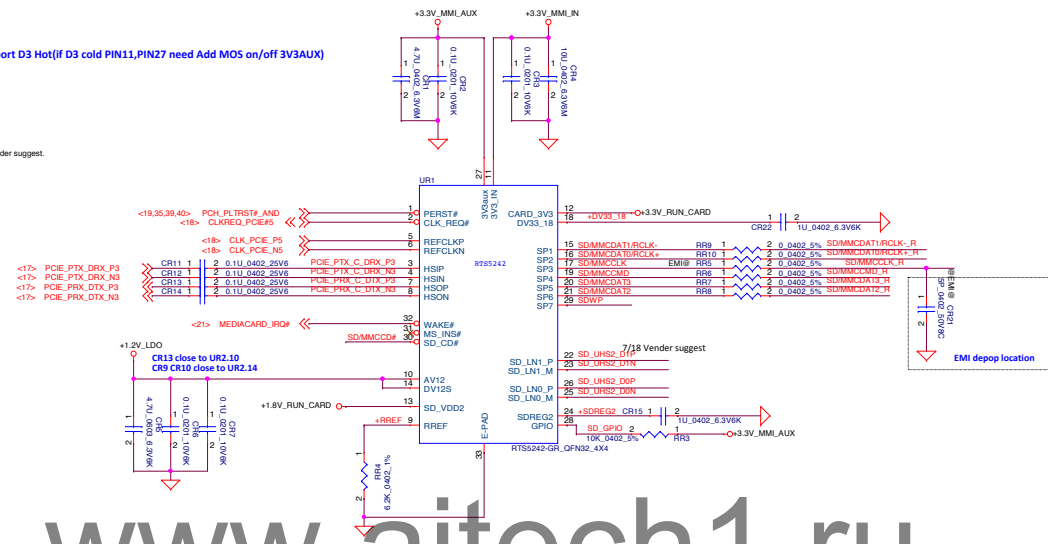
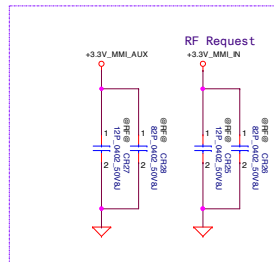
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| Security Classification | Compal Secret Data | | | Title | |
| Issued Date | 2016/01/01 | Deciphered Date | 2017/01/01 | Compal Electronics, Inc. eDP CONN & Touch screen | |
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| | | | | Number | 0.2 |
| | | | | LA-E151P | |
| Date: Tuesday, June 28, 2016 | | | | Sheet | 32 of 61 |

For PCIe Interface



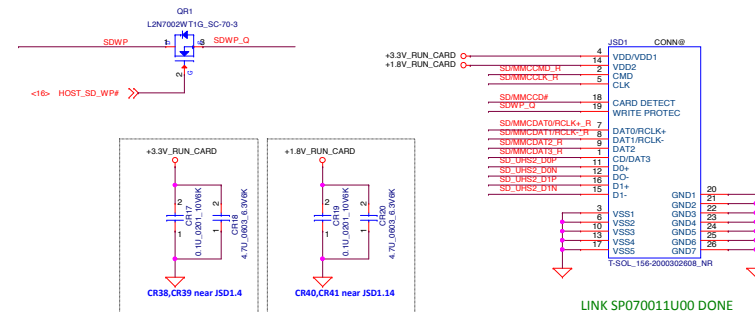
support D3 Hot(if D3 cold PIN11,PIN27 need Add MOS on/off 3V3AUX)

7/18 Vender suggest.



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| HOST_SD_WP# | SDWP_Q | SDWP | STATUS |
|-------------|--------|------|----------------------------|
| High | High | High | Write Protect(SD LOCK) |
| | Low | Low | Write Enable |
| Low | High | High | Write Protect(SD& FW LOCK) |
| | Low | High | Write Protect(FW LOCK) |



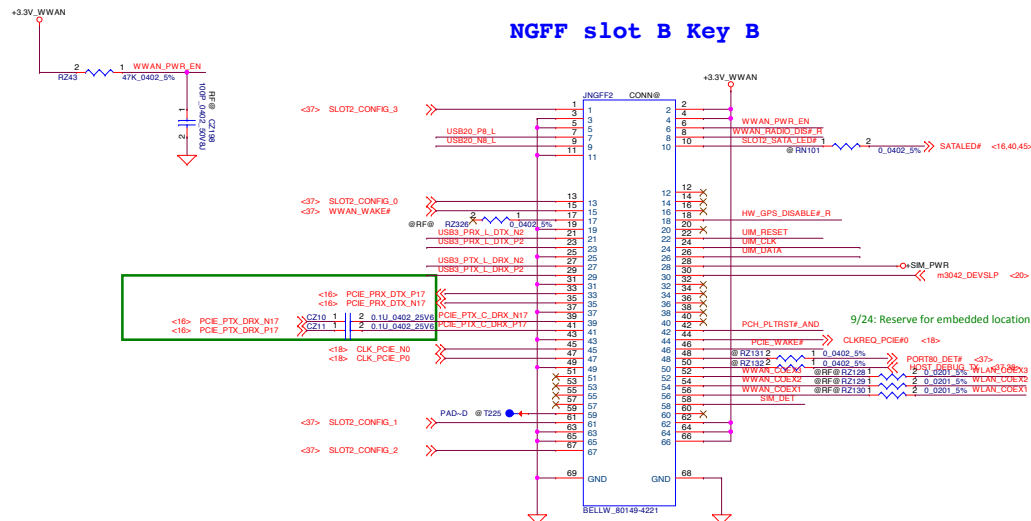
LINK SP070011U00 DONE

DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

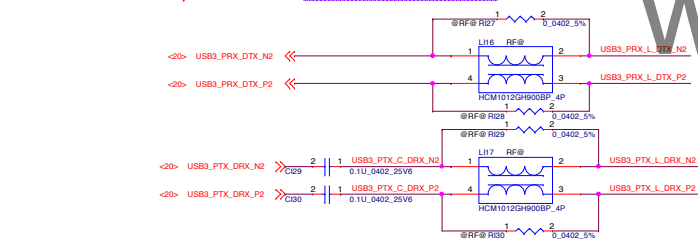
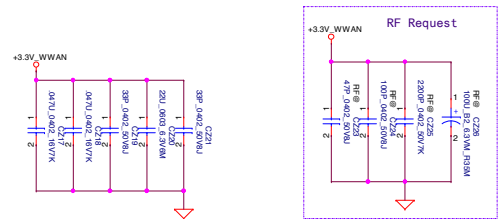
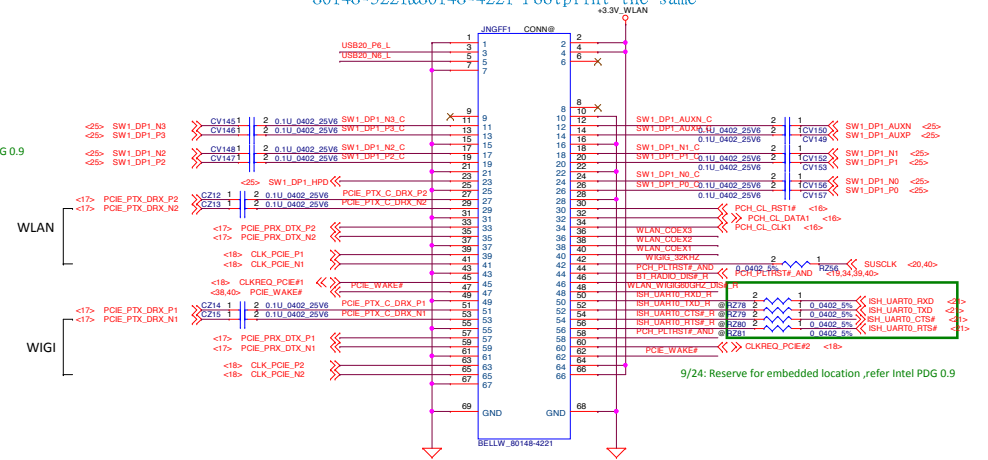
Card Reader

| | | | | | |
|--|------------------|--------------------|------------|---|--------------------|
| Security Classification | | Compul Secret Data | | DELETE CONFIDENTIAL/PROPRIETARY Compul Electronics, Inc. | |
| Issued Date | 2016/01/01 | Deciphered Date | 2017/01/01 | Title | Card Reader |
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| Date | January 29, 2016 | Issue | 34 | of | 61 |

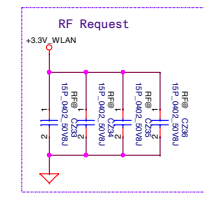
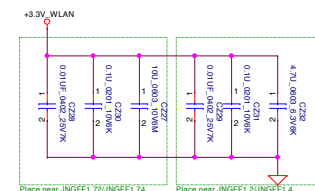
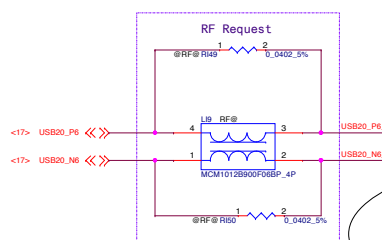
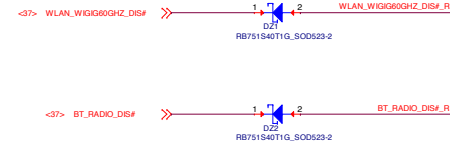
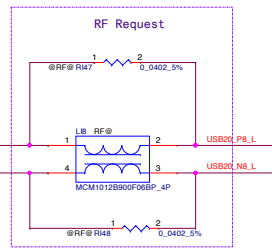
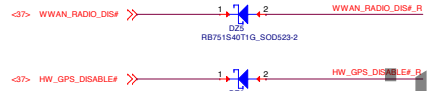
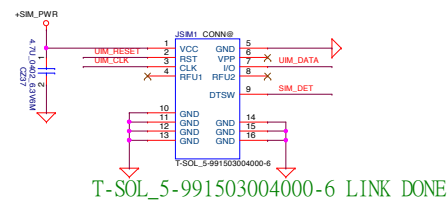


For TBT SW2_DP1
For non-TBT SW1_DP1

NGFF slot A Key A
80148-3221&80148-4221 Footprint the same



SIM Card Push-Push

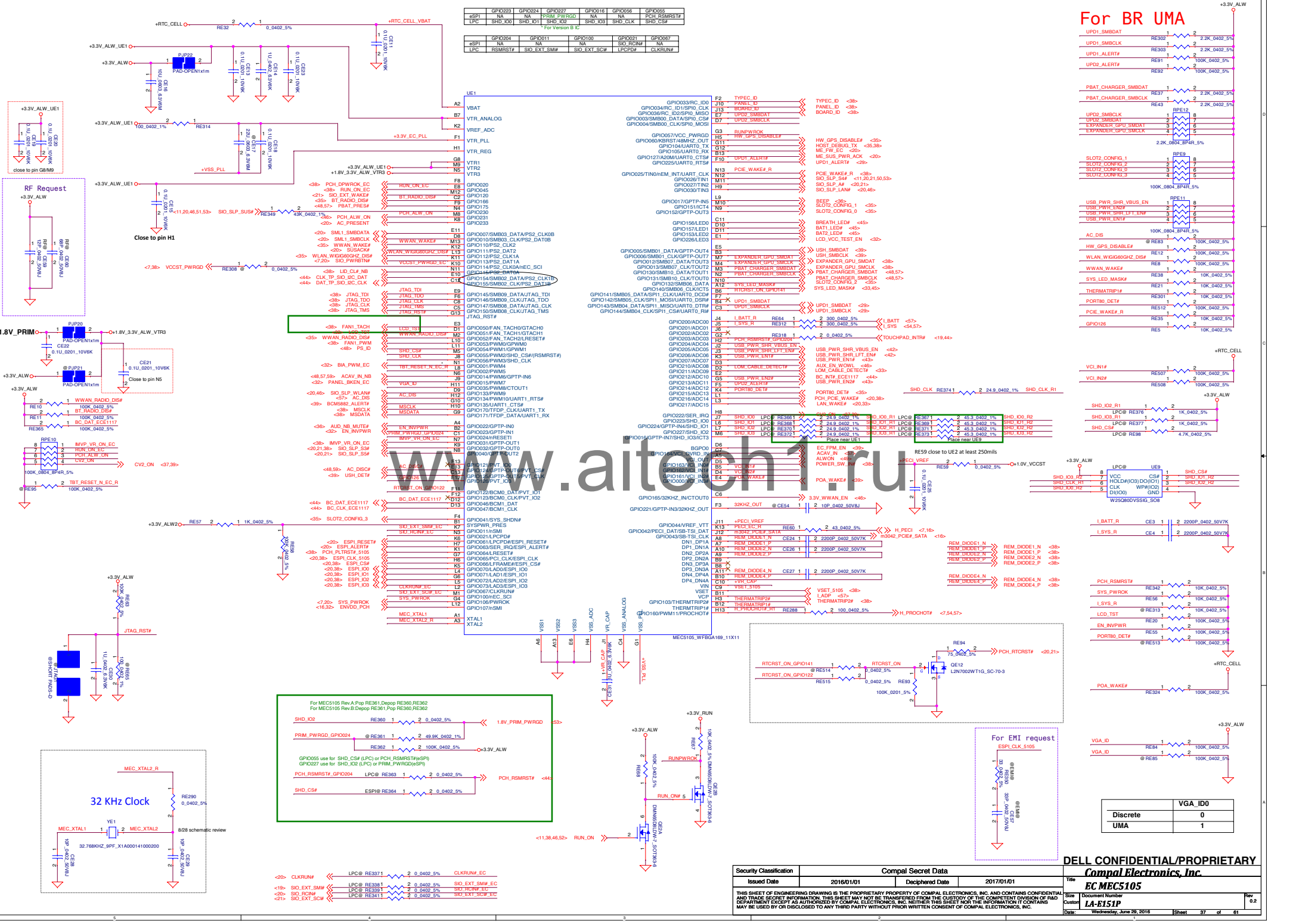


Power Rating TBD

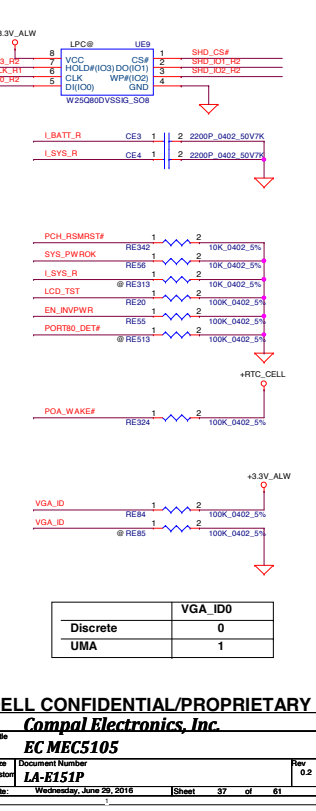
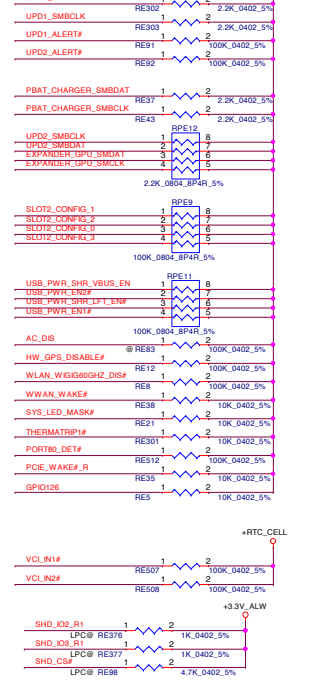
| PWR Rail | Voltage Tolerance | Primary Power | Aux Power |
|----------|-------------------|---------------|-----------|
| +3.3V | | Peak | Normal |

| STATE # | CONFIG_0 | CONFIG_1 | CONFIG_2 | CONFIG_3 | Module Type | m3042_PCIE#_SATA |
|---------|----------|----------|----------|----------|------------------|------------------|
| 0 | GND | GND | GND | GND | SSD-SATA | High |
| 1 | GND | HIGH | GND | GND | SSD-PCIe(2 lane) | Low |
| 8 | HIGH | GND | GND | GND | WWAN | Low |
| 14 | HIGH | GND | HIGH | HIGH | HCA-PCIe(1 lane) | Low |
| 15 | HIGH | HIGH | HIGH | HIGH | NA | Low |

| | | | | | |
|--|--------------|--------------------|------------|---|-----------------------------------|
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| Date: | July 9, 2018 | Sheet | 36 | of | 61 Rev 0.2 |



For BR UMA



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SECURITY CLASSIFICATION

Compal Secret Data

2016/01/01

Deciphered Date

2017/01/01

Document Number

EC M5C5105

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Size

Customer

LA-E151P

Date

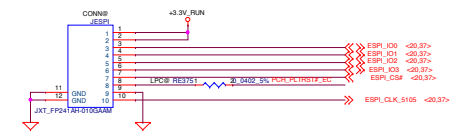
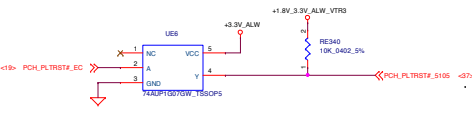
Wednesday, June 29, 2016

Sheet

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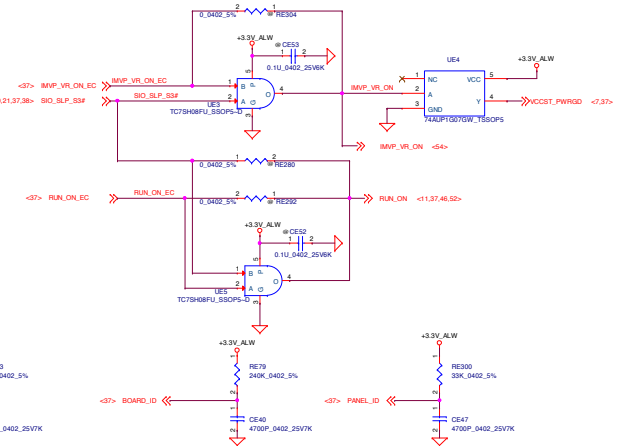
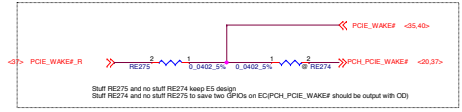
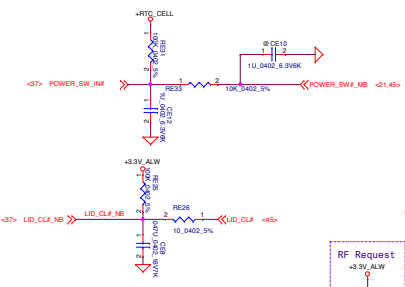
Rev

0.2



| LPC 80Port Debug | LPC | ESPI |
|------------------|-------------|-----------|
| 1 | +3.3V_RUN | +3.3V_RUN |
| 2 | +3.3V_RUN | +3.3V_RUN |
| 3 | LPC_LAD0 | ESPI_I00 |
| 4 | LPC_LAD1 | ESPI_I01 |
| 5 | LPC_LAD2 | ESPI_I02 |
| 6 | LPC_LAD3 | ESPI_I03 |
| 7 | LPC_FRAME# | ESPI_CS# |
| 8 | PCH_PLTRST# | NA |
| 9 | GND | GND |
| 10 | LPC_CLOCK | ESPI_CLK |

| PAGE | ESPI | LPC |
|------|--------------------|---|
| 8 | RC25_10K | RC8_15ohm RC18/RC27_8.2K |
| 18 | RC212_0ohm 0603 | RC211_0ohm 0603 |
| 31 | | RE337,RE338 RE339,RE340, RE341 0_ohm |
| 32 | RE2 / RE3 0_ohm | |



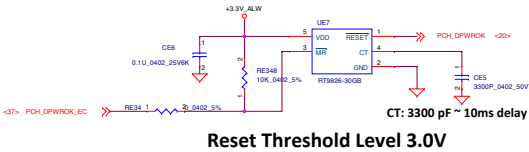
| RE343 | CE82 | REV |
|-------|-------|-------------------------------|
| 240K | 4700p | Single Port ACE w/o AR |
| 130K | 4700p | Single Port ACE w/AR |
| 62K | 4700p | Dual Port ACE w/o AR |
| 33K | 4700p | Dual Port ACE w/AR |
| 8.2K | 4700p | Dual Port ACE (w/AR + w/o AR) |
| 4.3K | 4700p | |
| 2K | 4700p | |
| 1K | 4700p | |

| RE79 | CE40 | REV |
|------|-------|-----|
| 240K | 4700p | X00 |
| 130K | 4700p | |
| 62K | 4700p | |
| 33K | 4700p | |
| 8.2K | 4700p | |
| 4.3K | 4700p | |
| 2K | 4700p | |
| 1K | 4700p | |

| RE300 | CE47 | PANEL SIZE |
|-------|-------|------------|
| 240K | 4700p | 12" |
| 130K | 4700p | 14" |
| 33K | 4700p | BR15 H |
| 4.3K | 4700p | BR15 P |

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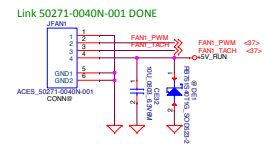
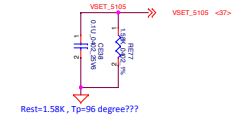
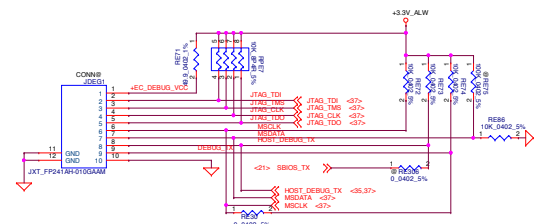
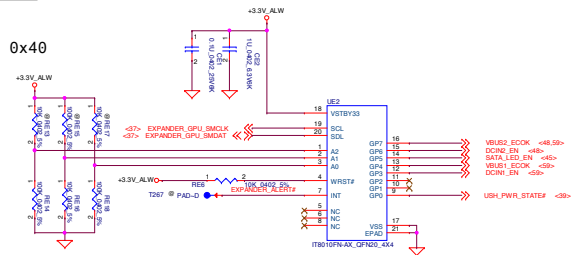
PD_ACE_DET# rise time is measured from 5%~68% BOARD_ID rise time is measured from 5%~68% PANEL_ID rise time is measured from 5%~68%



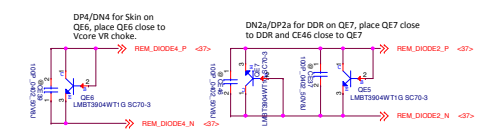
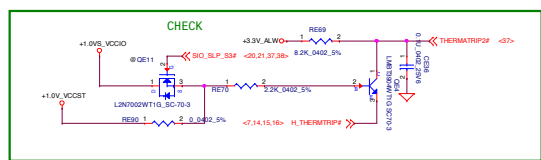
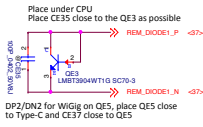
Reset Threshold Level 3.0V

| Control Byte |
|----------------------|
| 0 1 0 0 A2 A1 A0 R/N |
| R/N = 0 = Write |
| R/N = 1 = Read |

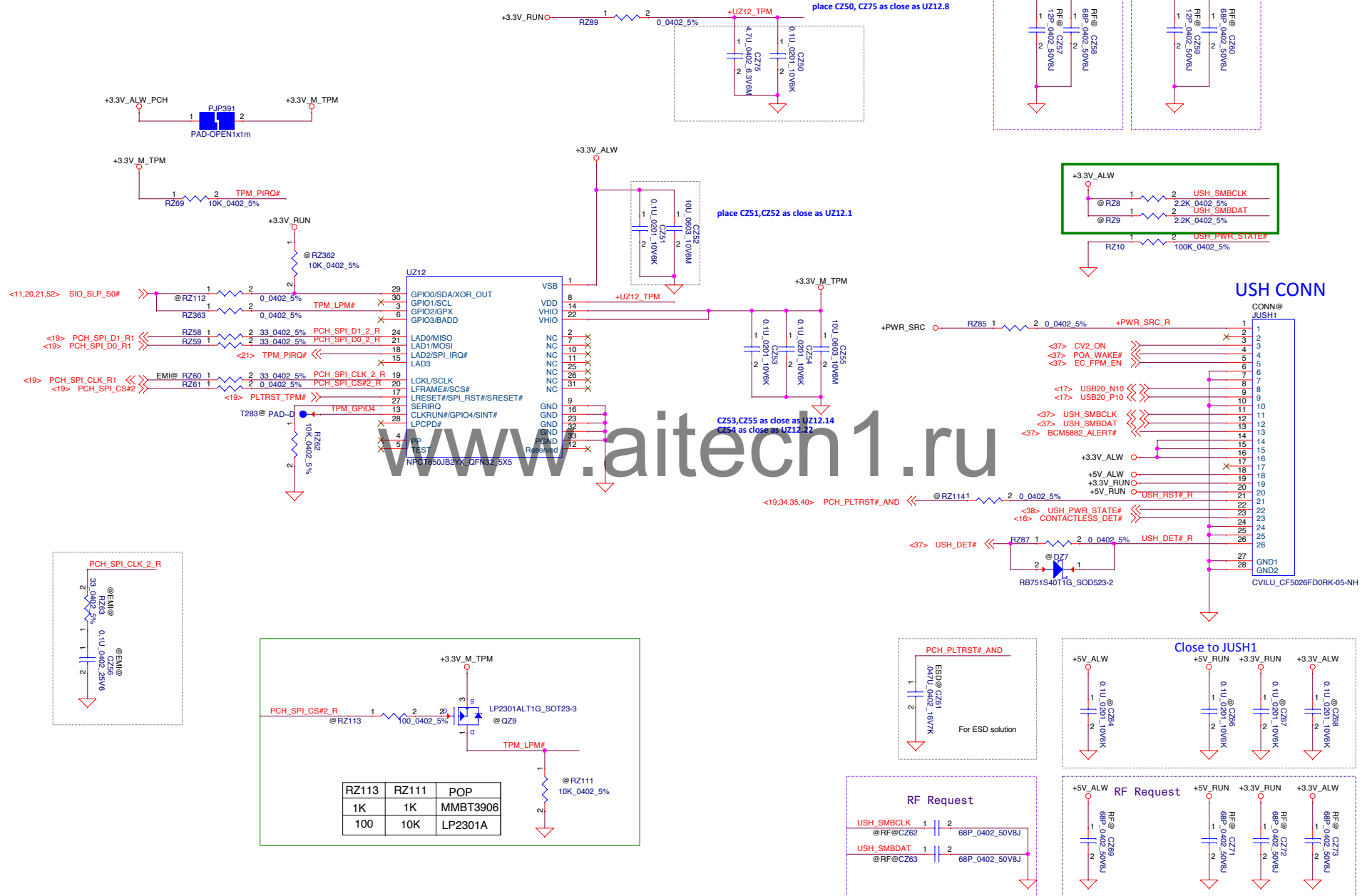
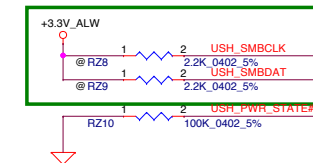
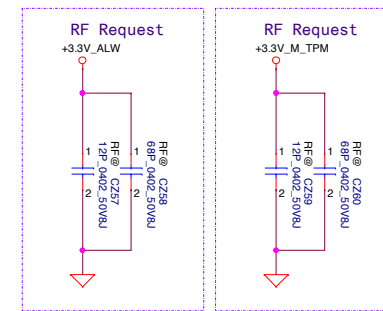
SMbus address 0x40



| 5105 Channel | Location |
|--------------|--------------|
| DP1/DN1 | CPU (QE3) |
| DP2/DN2 | WiGig (QE5) |
| DN2a/DP2a | DDR (QE7) |
| DP3/DN3 | NA |
| DP4/DN4 | CPU VR (QE6) |



For NUVOTON TPM



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USH & TPM

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| | USH & TPM | | |
| | Document Number | Rev | |
| Customer | LA-E151P | 0.2 | |
| Date: | Thursday, June 30, 2016 | Sheet | 30 of 61 |

RF Request

+3.3V_HDD_M2

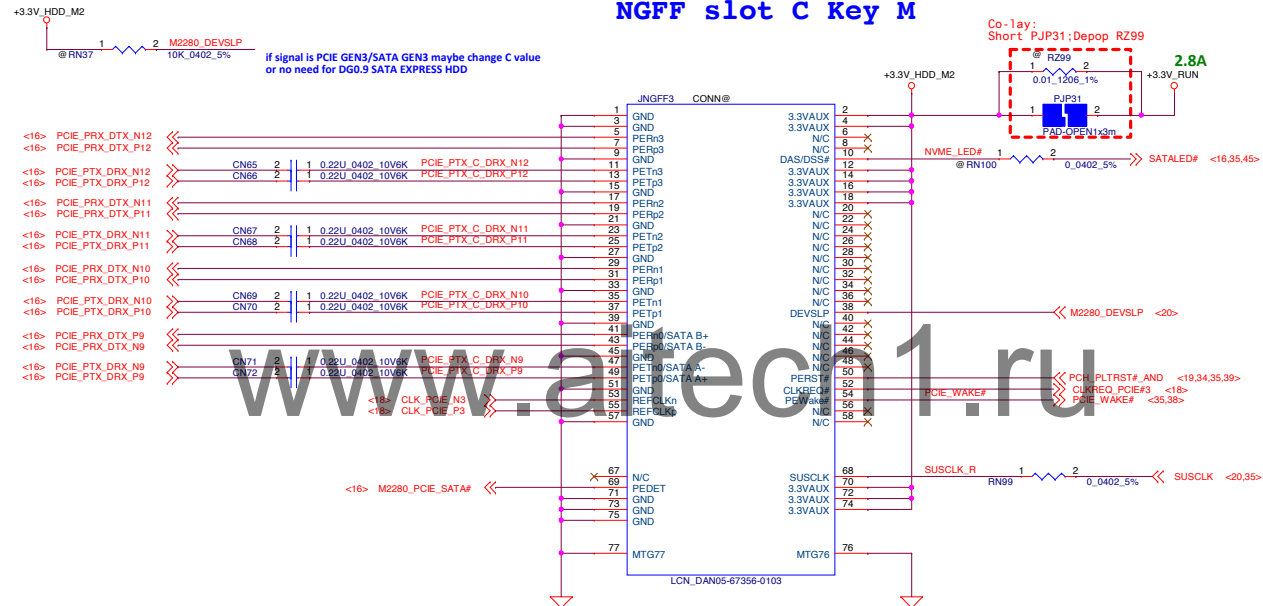
100pF @ 50V/181

100nF 0.003 50V/6A

220uF 0.003 5.0V/6A

Place near HDD CONN

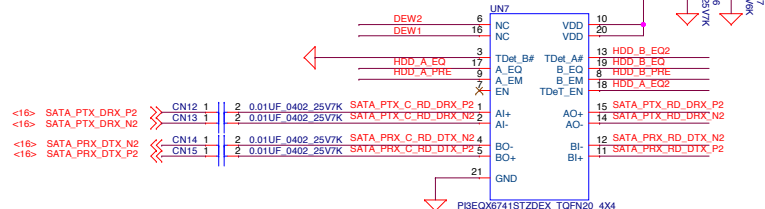
NGFF slot C Key M



| | | | | | |
|---|------------------------|--------------------|------------|--|--|
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| | | | | Document Number | 0.2 |
| | | | | LA-E151P | |
| Date | Tuesday, June 28, 2016 | Sheet | 40 | of | 61 |

| | pin 3 | pin 6 | pin 13 | pin 16 | pin 18 |
|----------------|---------|-------|---------|--------|---------|
| Pericom | TDet_B# | NC | TDet_A# | NC | TDet_EN |
| T1 | GND | DEW2 | GND | DEW1 | GND |
| Parade | GND | REXT | B_EQ2 | DEW | A_EQ2 |

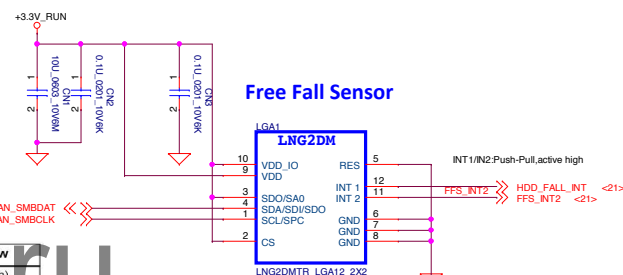
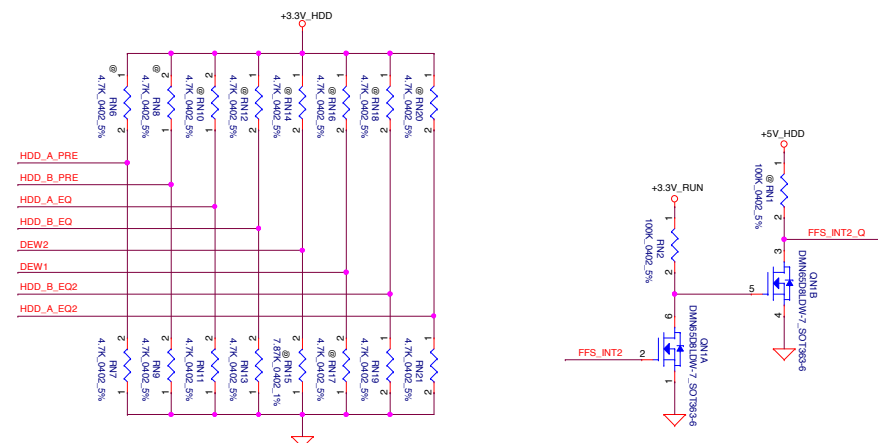
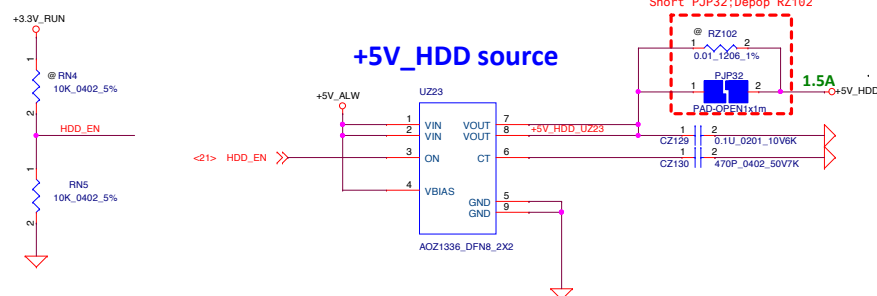
SATA Repeater



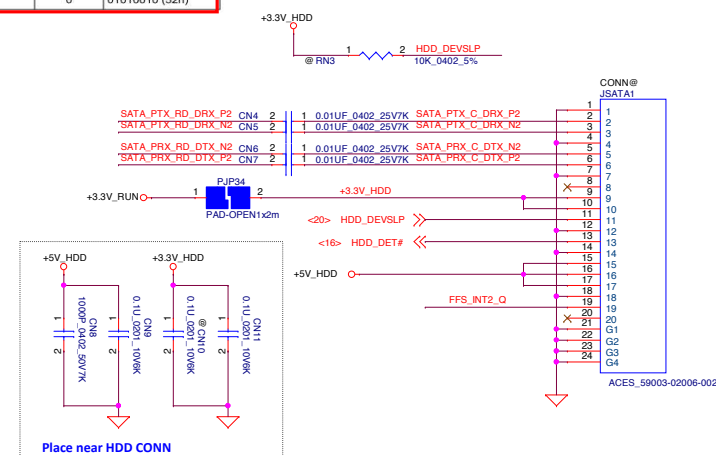
| | HDD_A_EO PIN17 | HDD_B_EO PIN19 | HDD_A_EO2 PIN18 | HDD_B_EO2 PIN13 | DEW1 PIN16 | DEW2 PIN6 | HDD_A_PRE PIN9 | HDD_B_PRE PIN8 |
|----------------------|-------------------|-------------------|--------------------|--------------------|-----------------|--------------|-------------------|-------------------|
| Pericom PI3EQX6741ST | PD (RN13) | PD (RN16) | PD (RN83) | PD (RD23) | NC | NC | PD (RN9) | PD (RN11) |
| TI SN75LVCP601 | PD (RN13) | NC | PD (RN83) | PD (RD23) | NC (1PU) | NC (1PU) | PH (RN8) | PH (RN10) |
| Parade PS8527C | PD (RN13) | PD (RN16) | PD (RN83) | PD (RD23) | NC (1/2 VDD) | PD (RN9) | NC (1/2 VDD) | NC (1/2 VDD) |

| | | | A_EQ | B_EQ | | A_EM | B_EM |
|------|---------|--------------|--------------------|--------------------|--------------|-------------------------|-------------------------|
| Main | Pericom | 0 NC 1 | 3dB 6dB 9dB | 3dB 6dB 9dB | 0 NC 1 | 0dB 1.5dB | 0dB 1.5dB |
| 2nd | TI | 0 NC 1 | 7dB 0dB 14dB | 7dB 0dB 14dB | 0 NC 1 | 0dB -4dB -2dB | 0dB -4dB -2dB |
| 3rd | Parade | EQ2 EQ1 | A_EQ | B_EQ | | A_EM | B_EM |
| | | (M = VDD/2) | | | | | |
| | | 0 M | 2.4dB | 2.4dB | 0 M 1 | 0dB -3.5dB -1.5dB | 0dB -3.5dB -1.5dB |
| | | 0 0 | 7.4dB | 7.4dB | | | |
| | | 0 1 | 14.4dB | 14.4dB | | | |
| | | M M | 12.2dB | 12.2dB | | | |
| | | M 0 | 9.4dB | 9.4dB | | | |
| | | M 1 | 13.3dB | 13.3dB | | | |
| | | 1 M | 6.2dB | 6.2dB | | | |
| | | 1 0 | 11.2dB | 11.2dB | | | |
| | | 1 1 | 5dB | 5dB | | | |

* red color is current setting



| Command | SAD[8:1] | SAD[0] = SA0 | R/W | SAD+R/W |
|---------|----------|--------------|-----|----------------|
| Read | 010100 | 0 | 1 | 01010001 (51h) |
| Write | 010100 | 0 | 0 | 01010000 (50h) |
| Read | 010100 | 1 | 1 | 01010011 (53h) |
| Write | 010100 | 1 | 0 | 01010010 (52h) |



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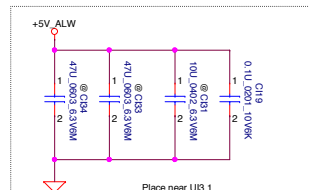
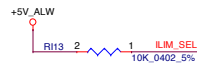
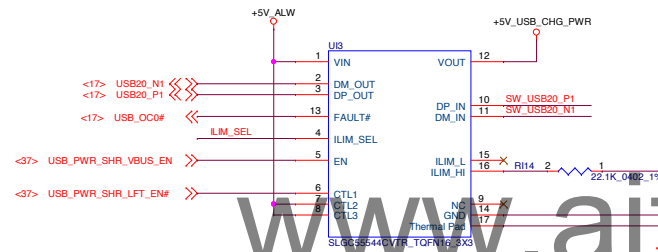
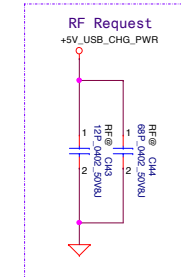
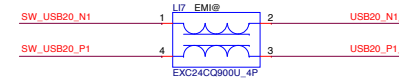
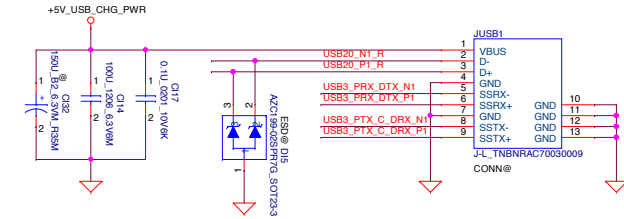
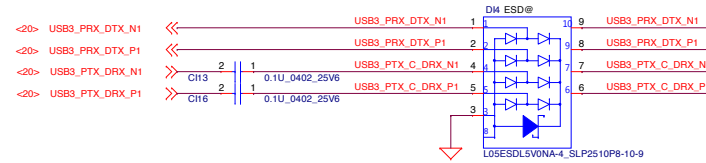
HDD CONN

| | | |
|------|-----------------|-----|
| Size | Document Number | Rev |
| B | LA-E151P | 0.2 |

| | | | | | |
|-------|------------------------|-------|----|----|----|
| Date: | Tuesday, June 28, 2016 | Sheet | 41 | of | 61 |
|-------|------------------------|-------|----|----|----|

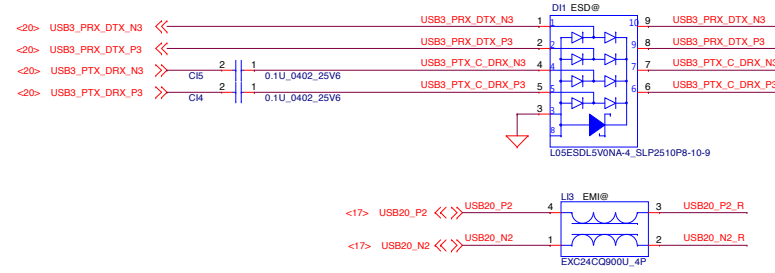
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For PWR SW + Charger combine IC

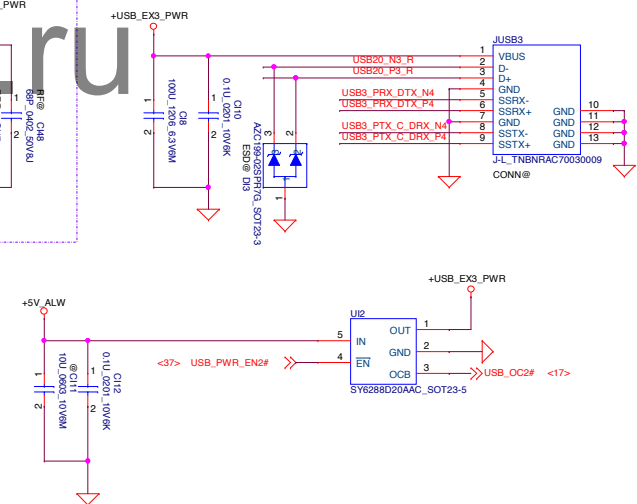
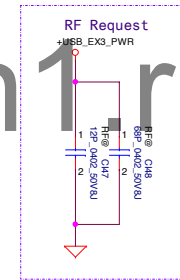
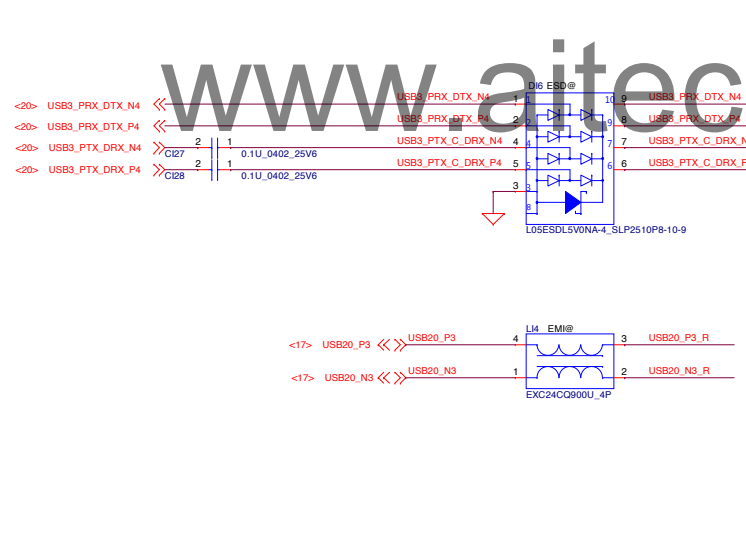
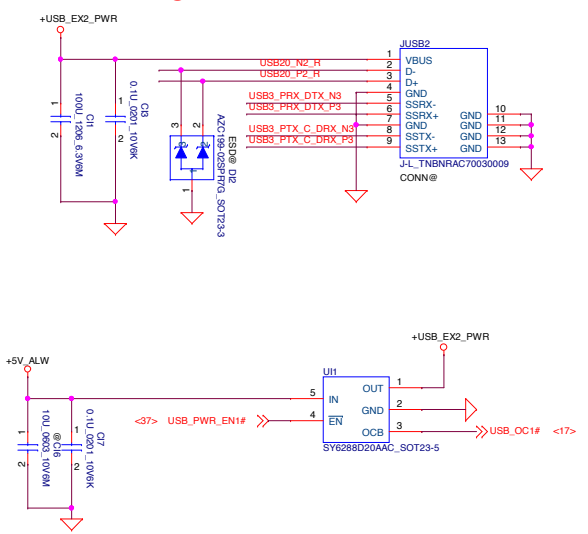
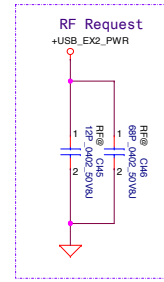


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| Sheet | | | | 42 | | | | of | | | |
| 61 | | | | | | | | | | | |

For Breckenridge 14&15/Steamboat 14



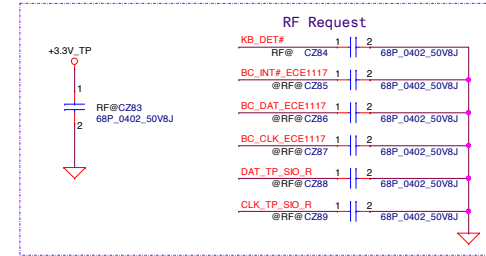
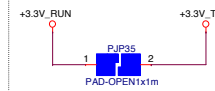
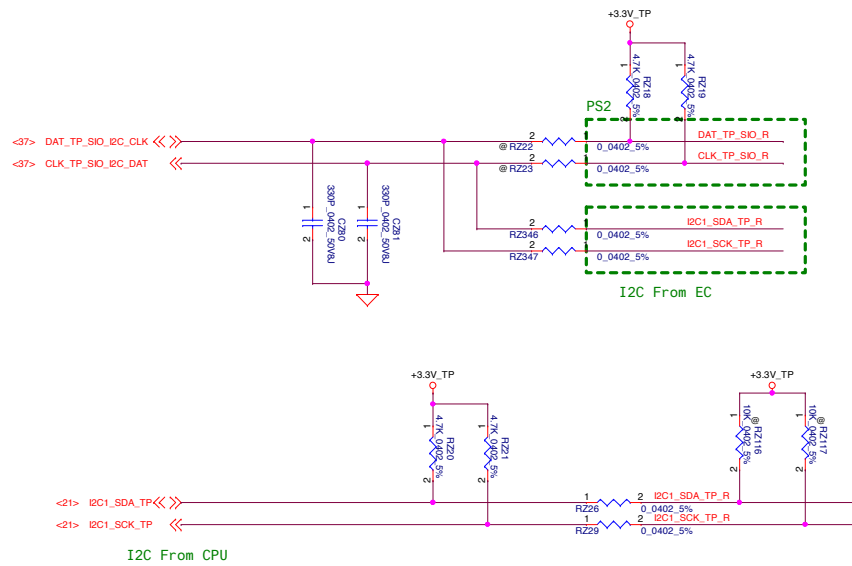
DfB request:
main SM070003200 (INPAQ_MCM1012B900F06BP_4P)
Footprint use 2nd source SM070004400 (PANAS_EXC24CQ900U_4P)
Pitch change from 0.5mm to 0.55mm



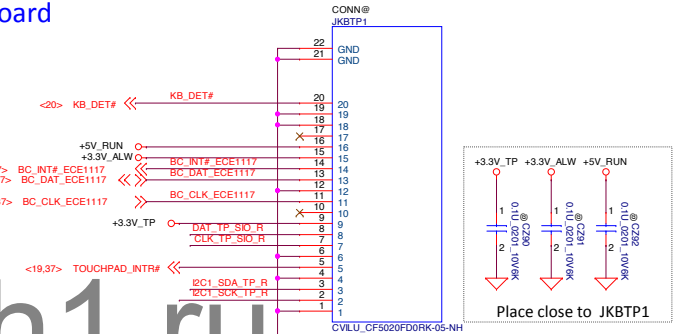
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|-------------------------------|------------------------|
| Compal Electronics, Inc. | |
| Title | JUSB2&JUSB3 |
| Document Number | LA-E151P |
| Date | Tuesday, June 28, 2016 |
| Sheet | 43 of 61 |

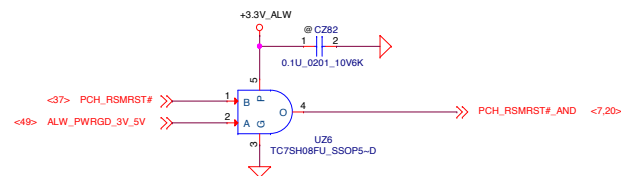
Touch Pad



Keyboard

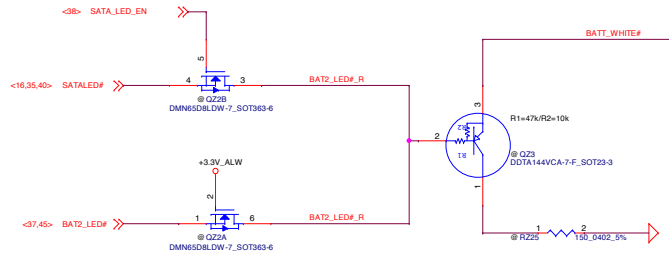


RSMRST circuit

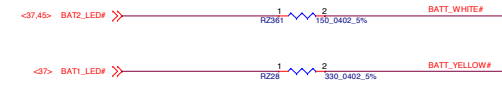


HDD LED MUX

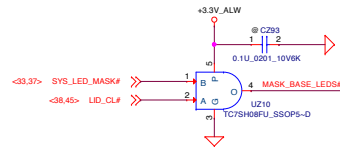
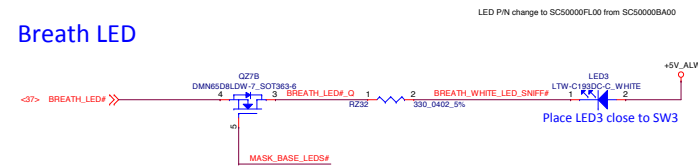
means EC can switch battery white led and HDD LED by hot key "Fn+H"



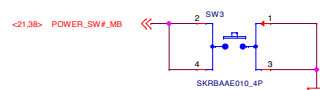
Battery LED



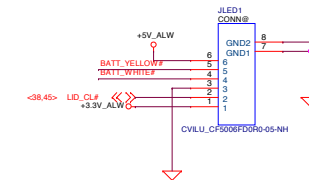
Breath LED



POWER & INSTANT ON SWITCH



LED board CONN

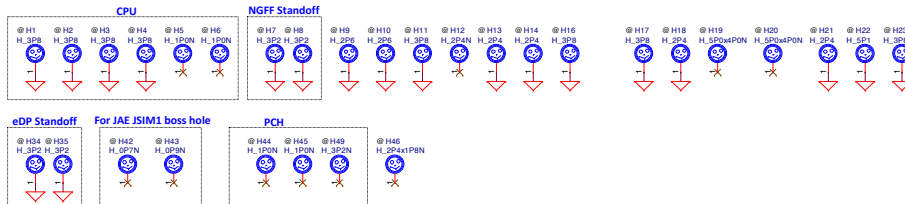


Fiducial Mark

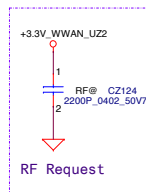
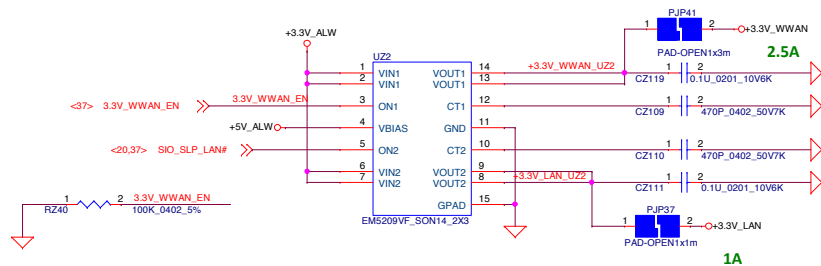


LED Circuit Control Table

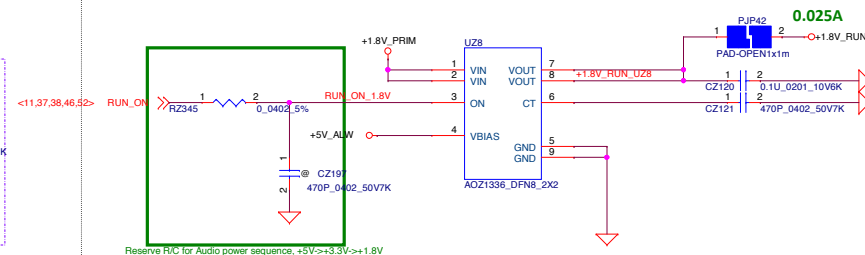
| | SYS_LED_MASK# | LID_CL# |
|----------------------------------|---------------|---------|
| Mask All LEDs (Unobtrusive mode) | 0 | X |
| Mask Base MB LEDs (Lid Closed) | 1 | 0 |
| Do not Mask LEDs (Lid Opened) | 1 | 1 |



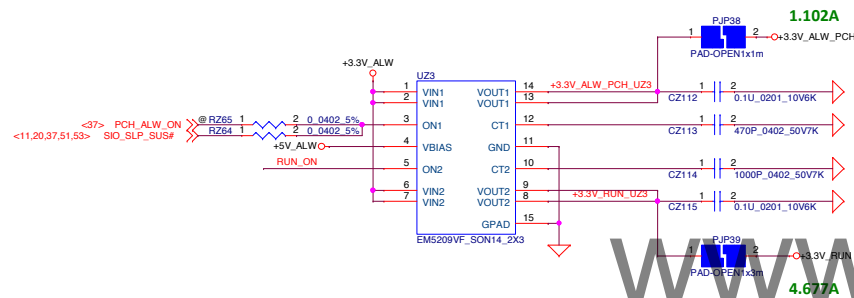
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+1.8V_RUN source

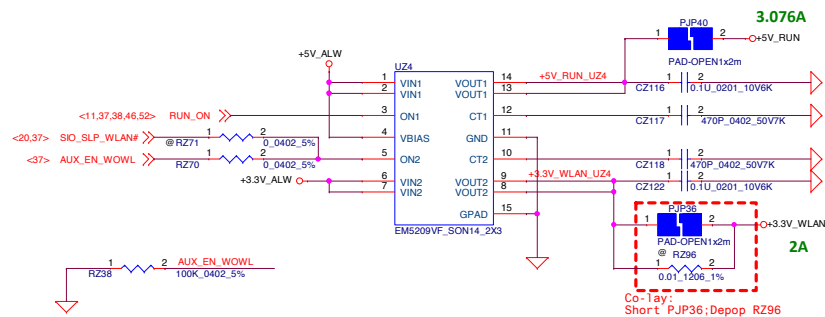


+3.3V_ALW_PCH/+3.3V_RUN source



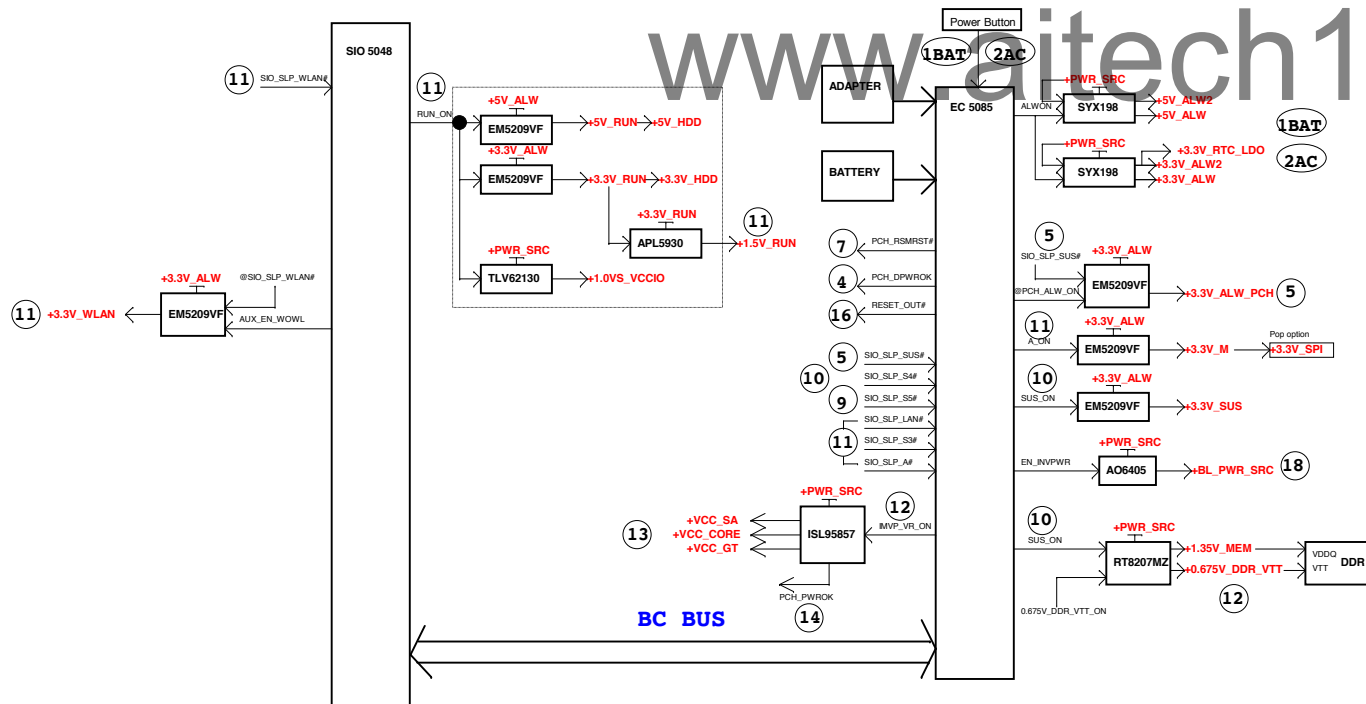
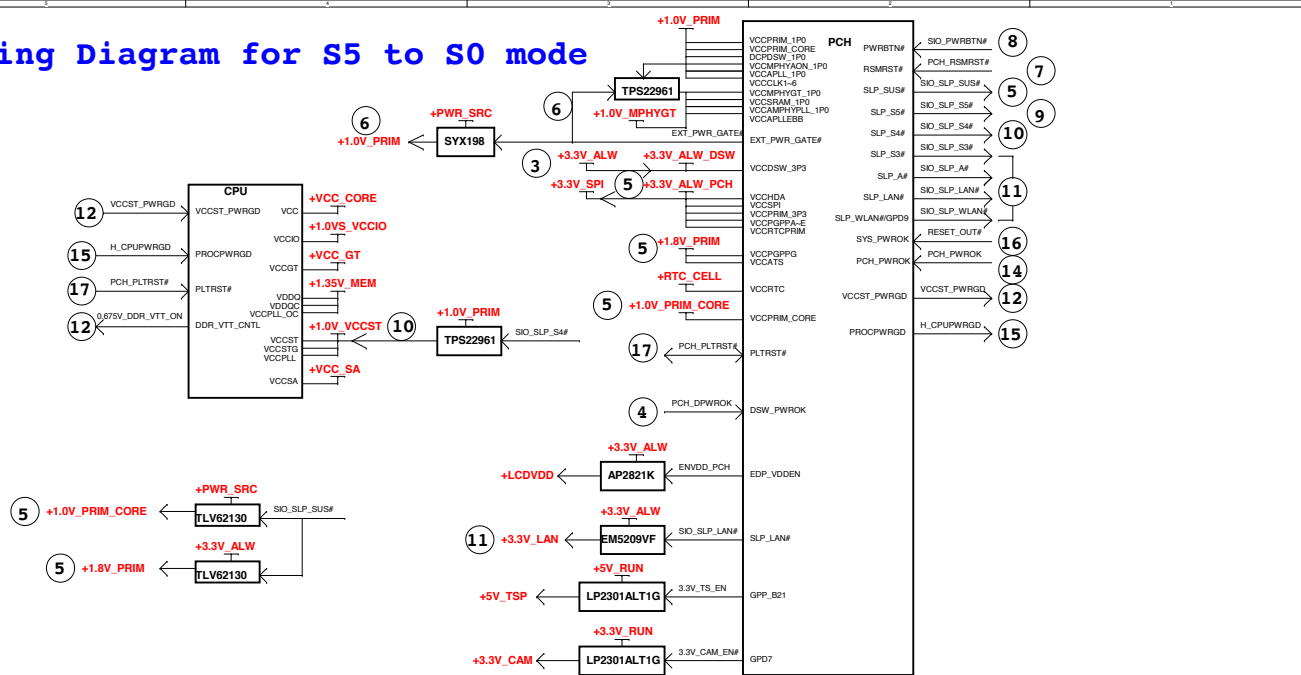
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+5V_RUN/+3.3V_WLAN source



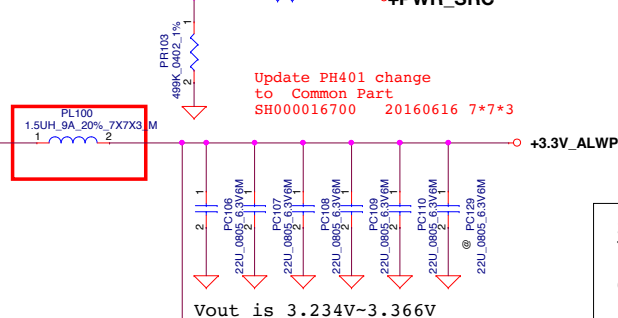
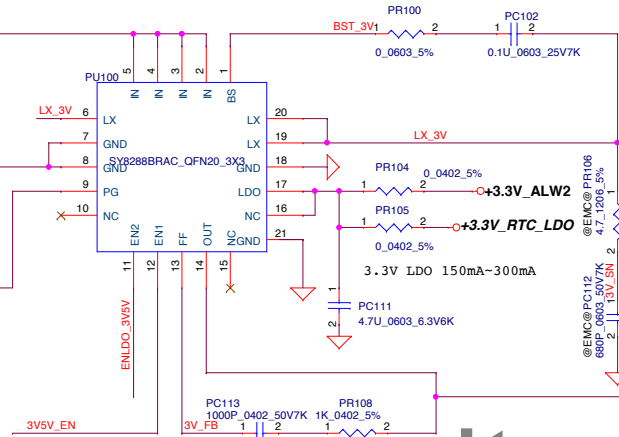
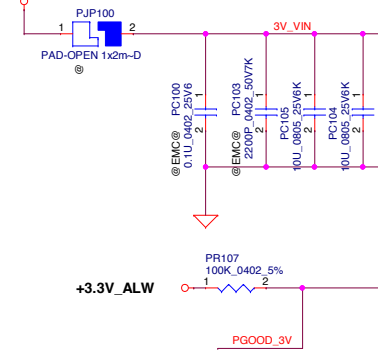
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| LA-E151P | | | | 0.2 | | | | Date: Tuesday, June 28, 2016 | | | |
| Sheet | | | | 46 | | | | of | | | |
| 61 | | | | | | | | | | | |

Timing Diagram for S5 to S0 mode

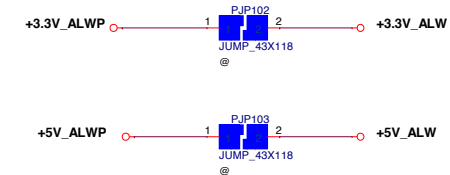


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| | | | Sheet 1 of 1 | |
| | | | Date 16-Jan-01 | |
| | | | Drawn by LA-ES1P | |
| | | | Date 16-Jan-01 | |
| | | | Issued by 47 of 61 | |

+PWR_SRC

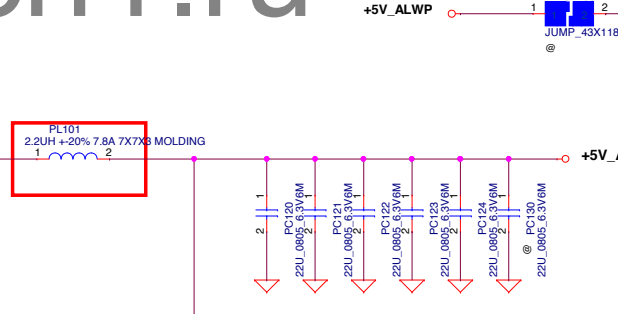
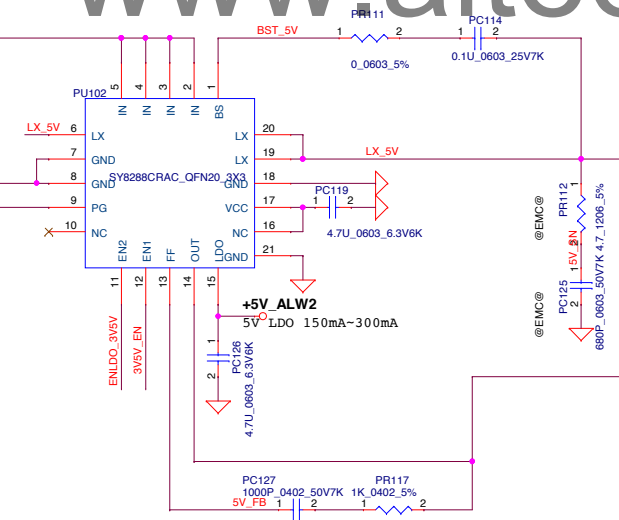
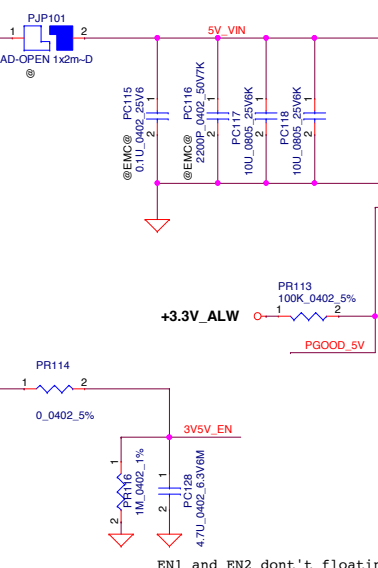


3VALWP
TDC 5.9 A
Peak Current 8.4 A
OCP Current 10.1 A



5VALWP
TDC 5.4 A
Peak Current 7.7 A
OCP Current 9.2 A

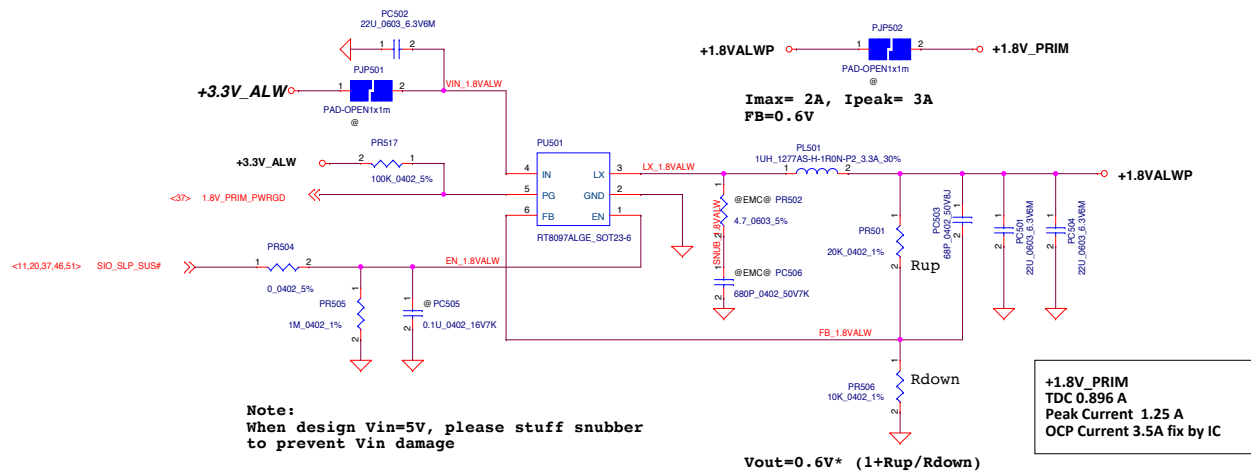
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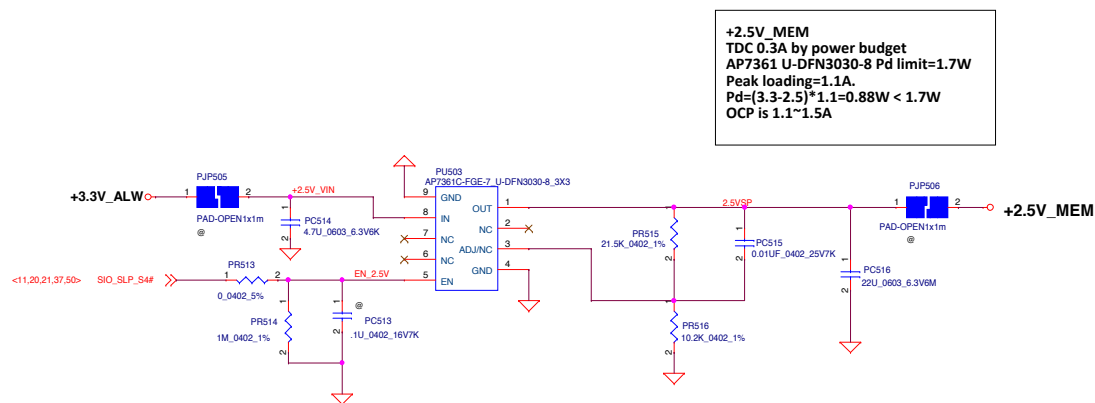
EN1 and EN2 don't floating

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| Sheet | | | 49 | | | of 61 | | |



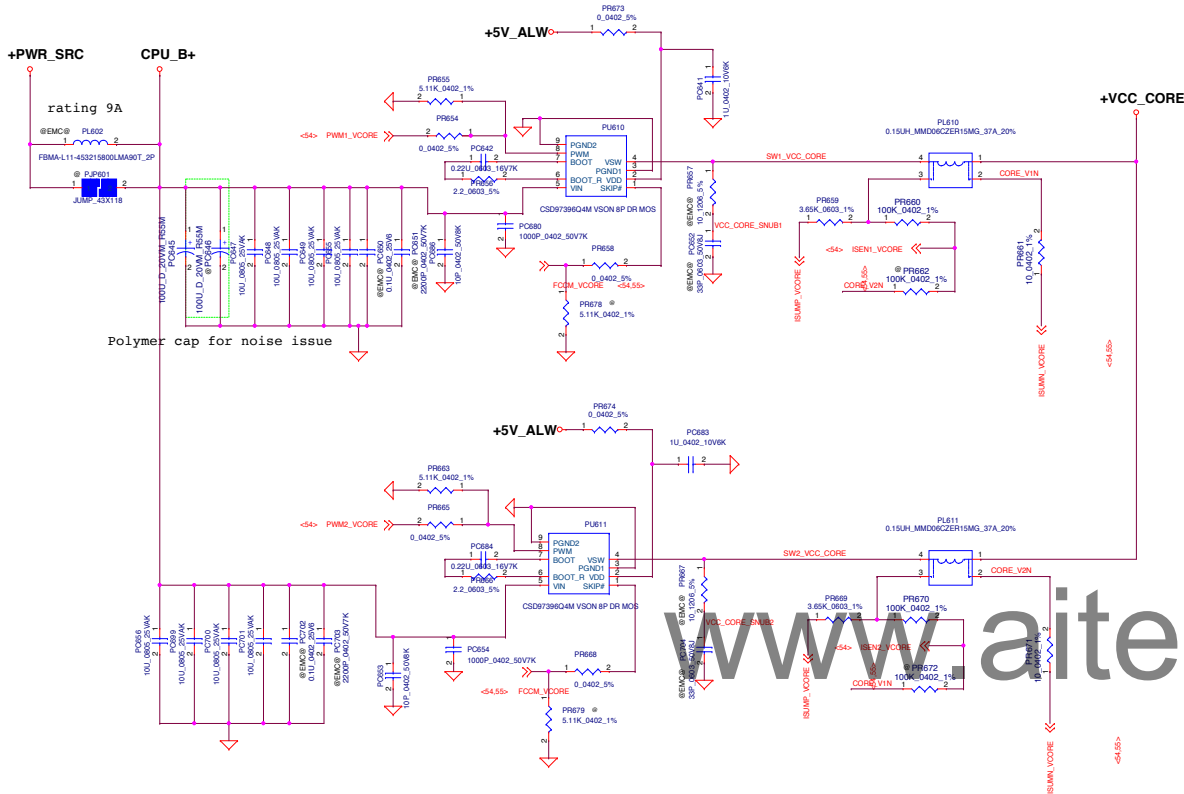
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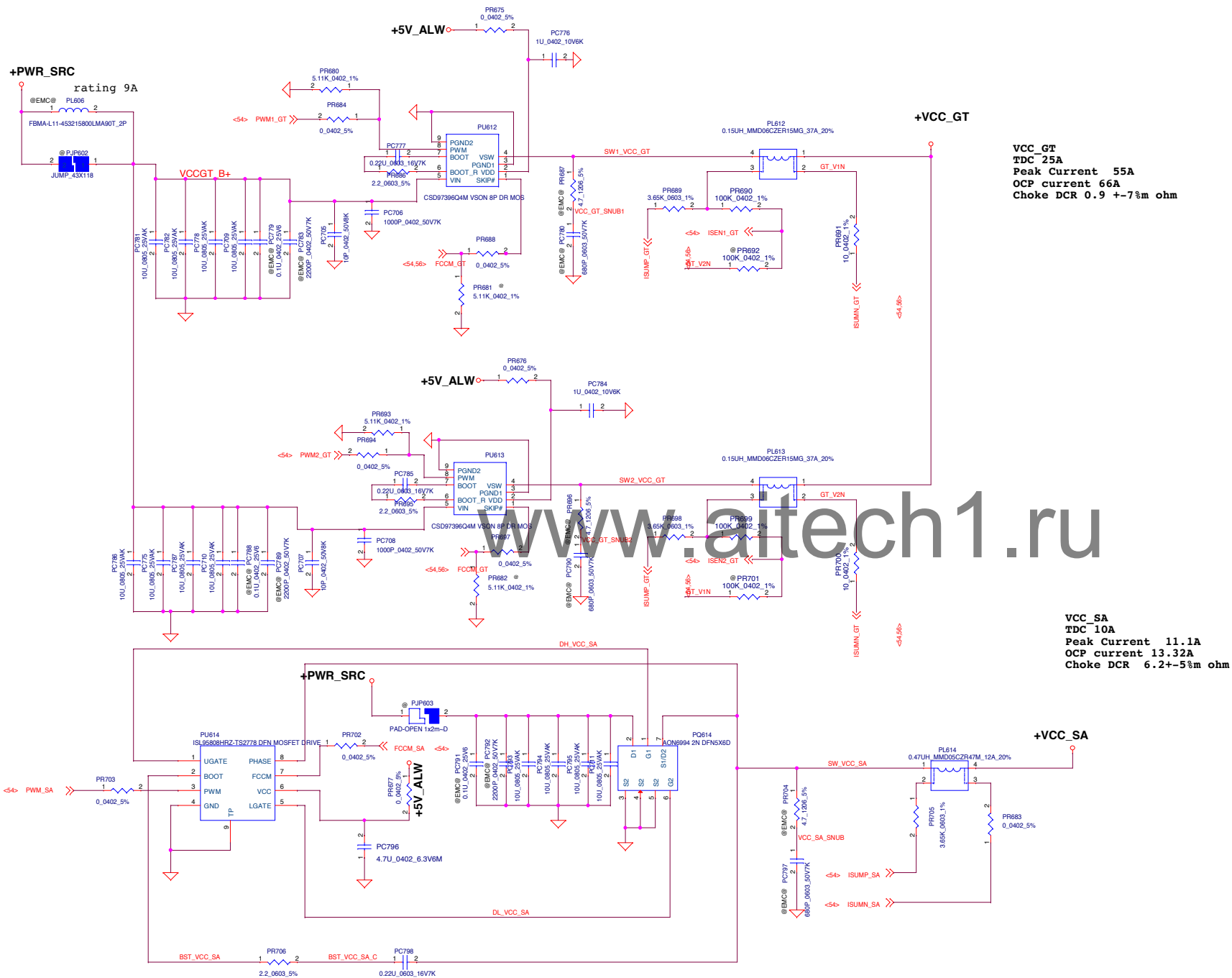
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| Compal Electronics, Inc. | | | |
| Title | +1.8VALWP/+1.5VSP / +2.5V_MEM | | |
| Size | Document Number | Rev | |
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VCC_core
TDC 50A
Peak Current 60A
OCP current 72A
Choke DCR 0.9 +-7% ohm



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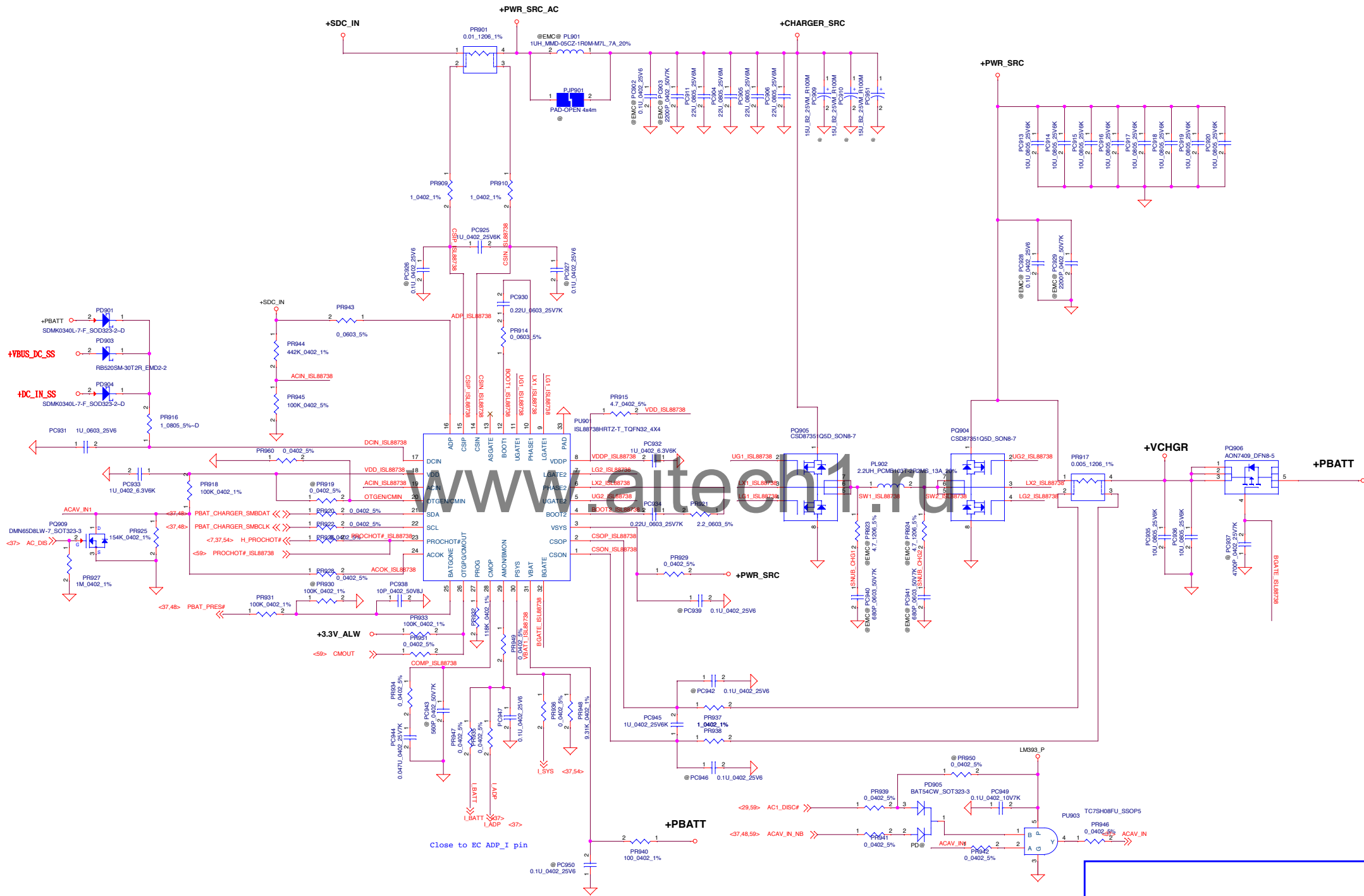
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| Title | | | | VCCORE | | | |
| Size | | Document Number | | Rev | | | |
| Custom | | LA-E151P | | Date | | Tuesday, June 28, 2016 | |
| | | Sheet | | 55 | | of 61 | |



VCC_GT
TDC 25A
Peak Current 55A
OCP current 66A
Choke DCR 0.9 +-7% ohm

VCC_SA
TDC 10A
Peak Current 11.1A
OCP current 13.32A
Choke DCR 6.2+-5% ohm

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| Size C | Document Number LA-E151P | Rev 0.2 | Date: Tuesday, June 28, 2016 Sheet 56 of 61 | |



Close to EC ADP_I pin

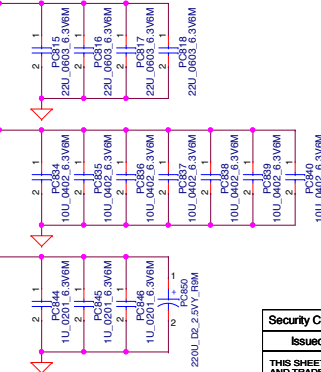
VCC_CORE Place on CPU
Back Side.
22U_0603 * 8 pcs + 10U_0402*28 pcs + 1U_0201*35 pcs
Primary Side.
22U_0603 * 8 pcs+330u_D2*2 pcs

+VCC_CORE



VCC_SA Place on CPU
Back Side.
22U_0603 * 2 pcs + 10U_0402*7 pcs + 1U_0201*3 pcs
Primary Side.
22U_0603 * 2 pcs + 220u_D2*1 pcs

+VCC_SA



VCC_GT Place on CPU
Back Side.
22U_0603 * 8 pcs +10U_0402*35 pcs +1U_0201*68 pcs
Primary Side.
22U_0603 * 12 pcs +470u_D2*2 pcs

+VCC_GT

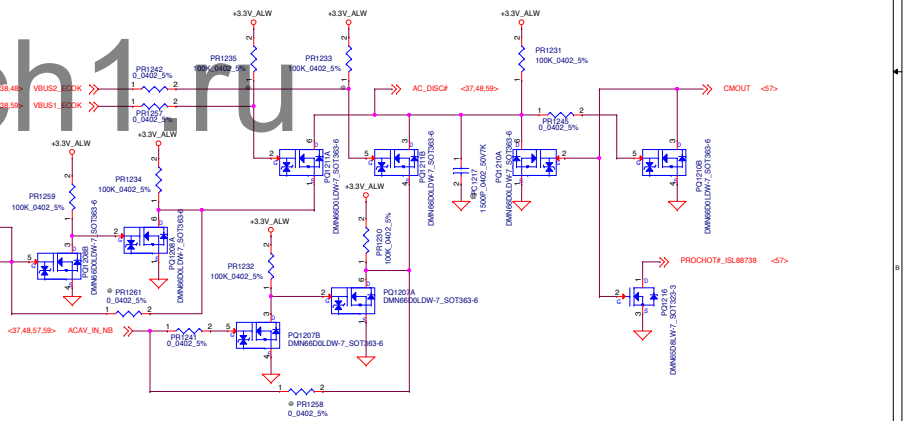
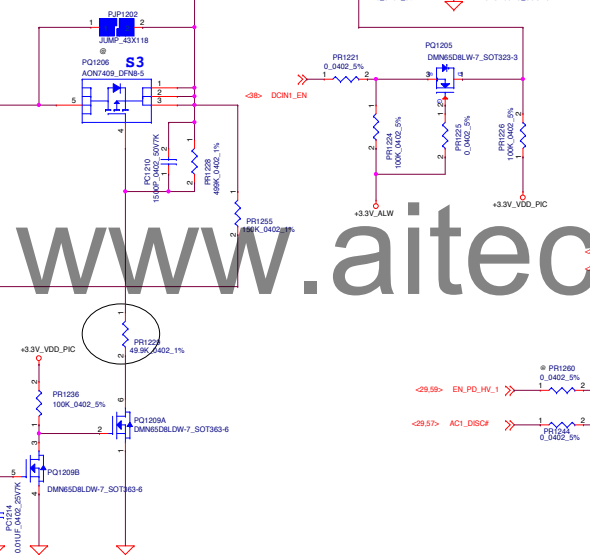
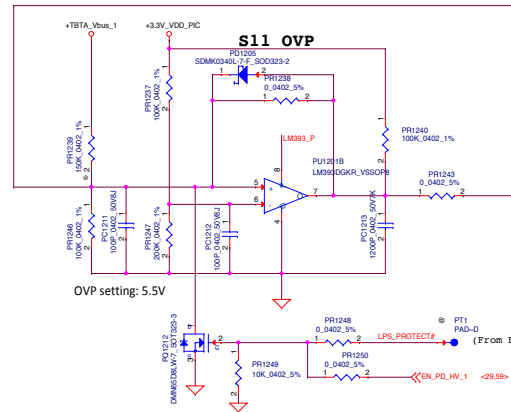
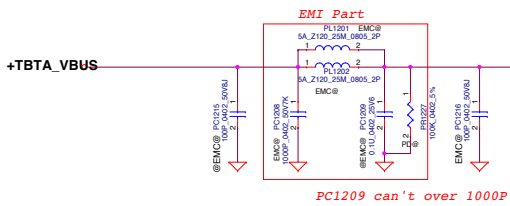
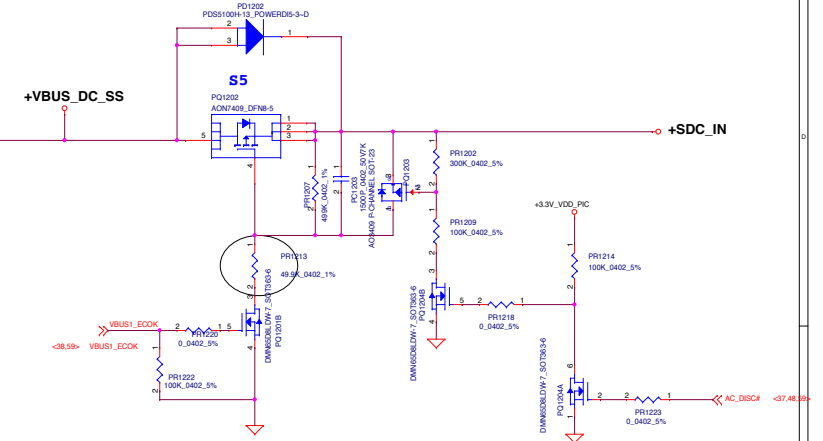
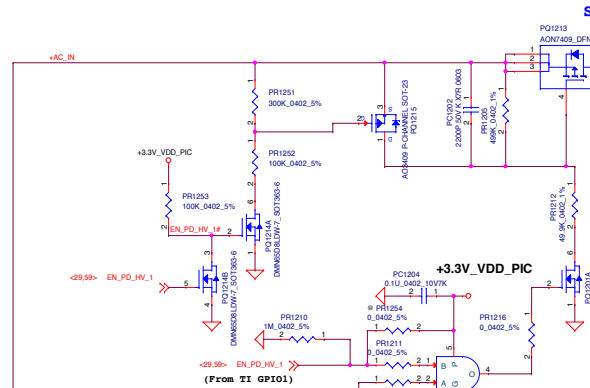
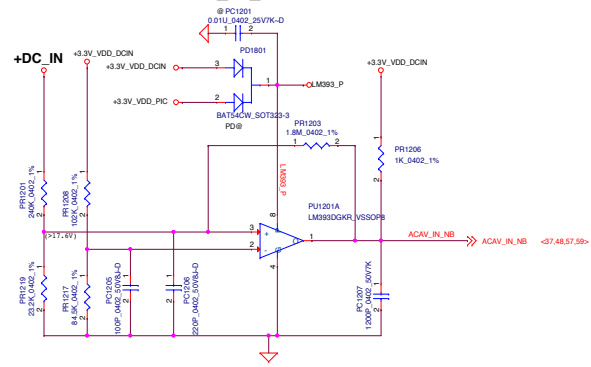


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PROCESSOR DECOUPLING

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| LA-E151P | | 02 |
| Date | Tuesday, June 28, 2016 | Sheet 58 of 61 |



Version Change List (P. I. R. List)

| Item | Page# | Title | Date | Request Owner | Issue Description | Solution Description | Rev. |
|------|-------|-------|------|---------------|-------------------|----------------------|------|
| 1 | | | | | | | |
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Version Change List (P. I. R. List)

| Item | Page# | Title | Date | Request Owner | Issue Description | Solution Description | Rev. |
|------|-------|-------|-----------|---------------|---|---|----------|
| 1 | 11 | HW | 2016/5/27 | COMPAL | S0ix(modern standby) support for VCCPLL_OC | Pop RZ120 and Depop UZ34 Add net name VCCSTG_EN(UZ19.4) and connect to RZ120.1 | 0.2(X01) |
| 2 | 37 | HW | 2016/5/27 | COMPAL | Reserve PORT80_DET# PD resistance | Reserve RE513 100k (SD028100380) to GND | 0.2(X01) |
| 3 | 35 | HW | 2016/6/1 | COMPAL | Intel schematics reivew modify item | CZ28,CZ29 change from 0.047uF to 0.01uF CZ27 change from 0.1uF(@)_0201 to 10uF_0603 | 0.2(X01) |
| 4 | 45 | HW | 2016/6/1 | COMPAL | JLED1 pin define error | JLED1 pin definition change | 0.2(X01) |
| 5 | 39 | HW | 2016/6/1 | COMPAL | TPM change to NUVOTON | Change TPM from Atmel to NUVOTON. | 0.2(X01) |
| 6 | 35 | HW | 2016/6/1 | COMPAL | Intel reviwie result (WWAN Coex feature support) | Add RZ128 0 ohm connect WWAN_COEX3 and WLAN_COEX3 Add RZ129 0 ohm connect WWAN_COEX2 and WLAN_COEX2 Add RZ130 0 ohm connect WWAN_COEX1 and WLAN_COEX1 | 0.2(X01) |
| 7 | 35 | HW | 2016/6/7 | COMPAL | Debug card reserve | Add RZ131, RZ132 for PORT80_DET# and HOST_DEBUG_TX | 0.2(X01) |
| 8 | 37 | HW | 2016/6/7 | COMPAL | For MEC5105K-D1-TN setting | 1. Change UE1 to SA00009GL00 2. POP RE360,RE362 3. De-POP RE361 | 0.2(X01) |
| 9 | 35,32 | HW | 2016/6/16 | COMPAL | For EMC request | De-pop RZ131, RZ132. CL22 change to 10pf , POP CA7,CZ1 (100P),CH268 modify from 22p to 47p and POP,Change LV1 to SM01000NY00 | 0.2(X01) |
| 10 | 41 | HW | 2016/6/16 | COMPAL | BITS284924-HDD is still working after press power button into S5 during POST. | POP RN5 | 0.2(X01) |
| 11 | 39 | ME | 2016/6/17 | COMPAL | Connector change | 1. JKBTP1 change to CVILU CF5020FD0RK-05-NH 2. JUSH1 change to CVILU CF5026FD0RK-05-NH 3. JIR1 change to ACES_50208-0060N-P01 | 0.2(X01) |
| 12 | 36 | HW | 2016/6/20 | COMPAL | Vender suggest | RA7,RA8 change to 16.2ohm | 0.2(X01) |
| 13 | 37 | HW | 2016/6/22 | COMPAL | The possibility of GPIO map update | Add RE514,RE515 for RTCRST_ON | 0.2(X01) |
| 14 | 41 | HW | 2016/6/22 | COMPAL | BITS283552 - [BR_CSLP] FFS AP no function when execute FF generator or shake SU | FFS VDD_IO change to +3.3V_RUN | 0.2(X01) |
| | | | | | | | |

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| | | | | Revision Date | Revision Date |
| | | | | Tuesday, June 28, 2016 | Sheet 61 of 61 |